

Cover Sheet	1
Block Diagram	2
Clock Distribution	3
Power Delivery Map	4
Power On Sequence	5
Reset/power good	6
STRAP	7
CPU 1-6	8-13
DDR3-1:CHA	14
DDR3-2:CHB	15
PCIE X16	16
Clock Gen	17
PCH 1-8	18-25
VGA	26
DVI	27
PCIE 1X	28
AUDIO_ALC662/VT1705CE	29
AUDIO CONN/SPDIF/CD-IN	30
LAN_AR8161/AR8162	31
LAN/USB2.0 CONN	32
Front USB2.0 Header	33
SIO-NCT5573D	34
PS2/FAN	35
TPM/LPT/COM	36
ATX CONN/FP PANEL/RSMRST	37
1D05/1D8V/VCCSA	38
5V_DUAL/3.3V_SB/3.3V_DUAL	39
1D5V_STR	40
CPU_VCCIO	41
VCORE/AXG PWM	42
VCORE/AXG DRIVER	43
XDP	44
THROUGH HOLE	45
Changelist	46

H61M06

Fab A

Micro ATX 8.9X6.8

CPU:

Intel Sandy Bridge processors in LGA1155 Package

System Chipset:

PCH

Main Memory:

Dual Channel / DDR-III * 2 (Max 8GB)

On Board Device:

SIO: IT8772

LAN: RelTek RTL8111F/8105E

HDA Codec: ALC662

BIOS:SPI Flash ROM 4Mbyte

Expansion Slots:

PCI EXPRESS 16X SLOT *1


PCI EXPRESS 1X SLOT * 2

H61MXE-S USB3+RTL8111F+POWER MOS+Solid CAP

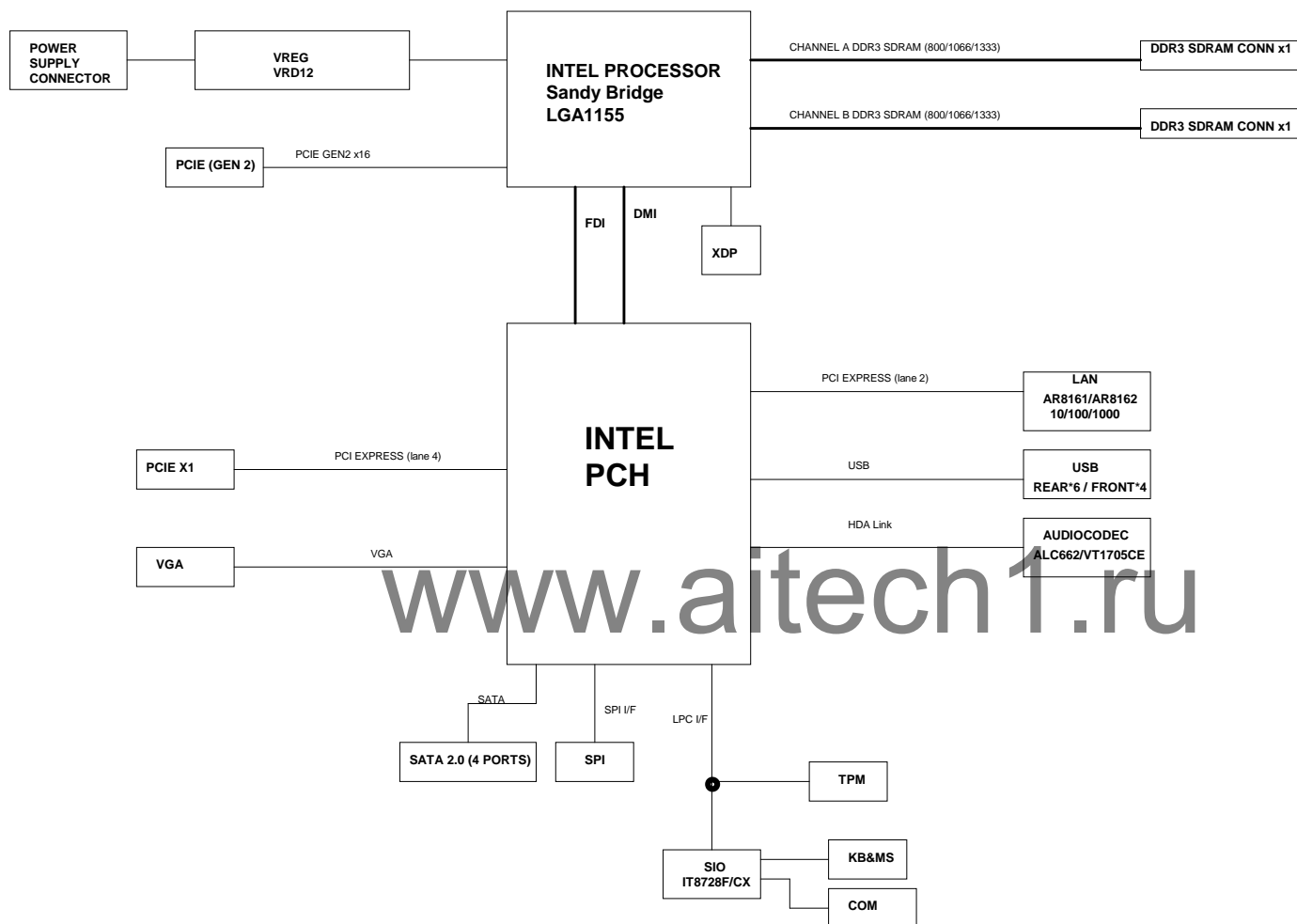
H61MXE RTL8111F

H61MXE-V RTL8105E

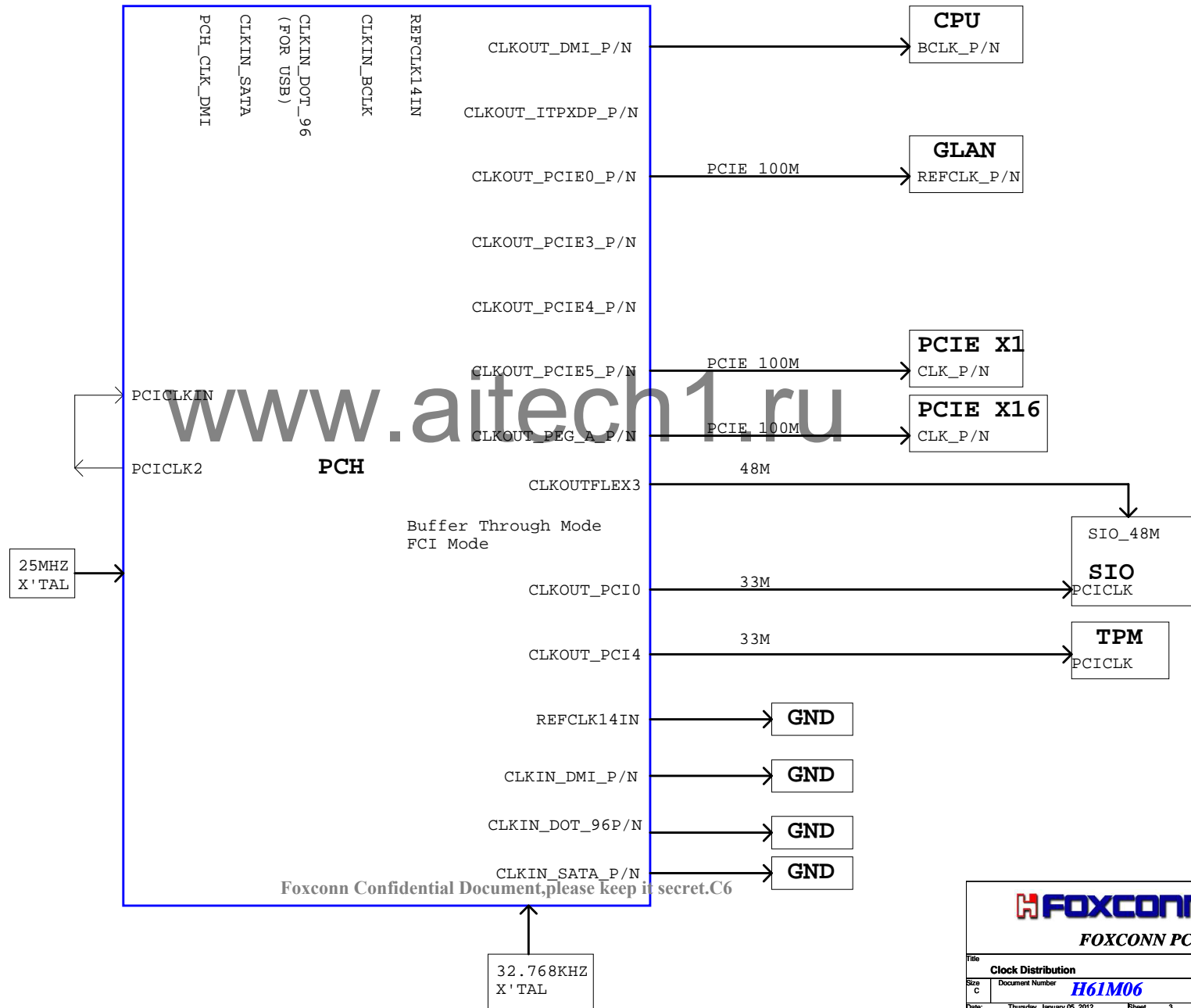
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Title		
Cover Sheet		
Size	Document Number	Rev
C	H61M06	A
Date:	Thursday, January 05, 2012	Sheet 1 of 45

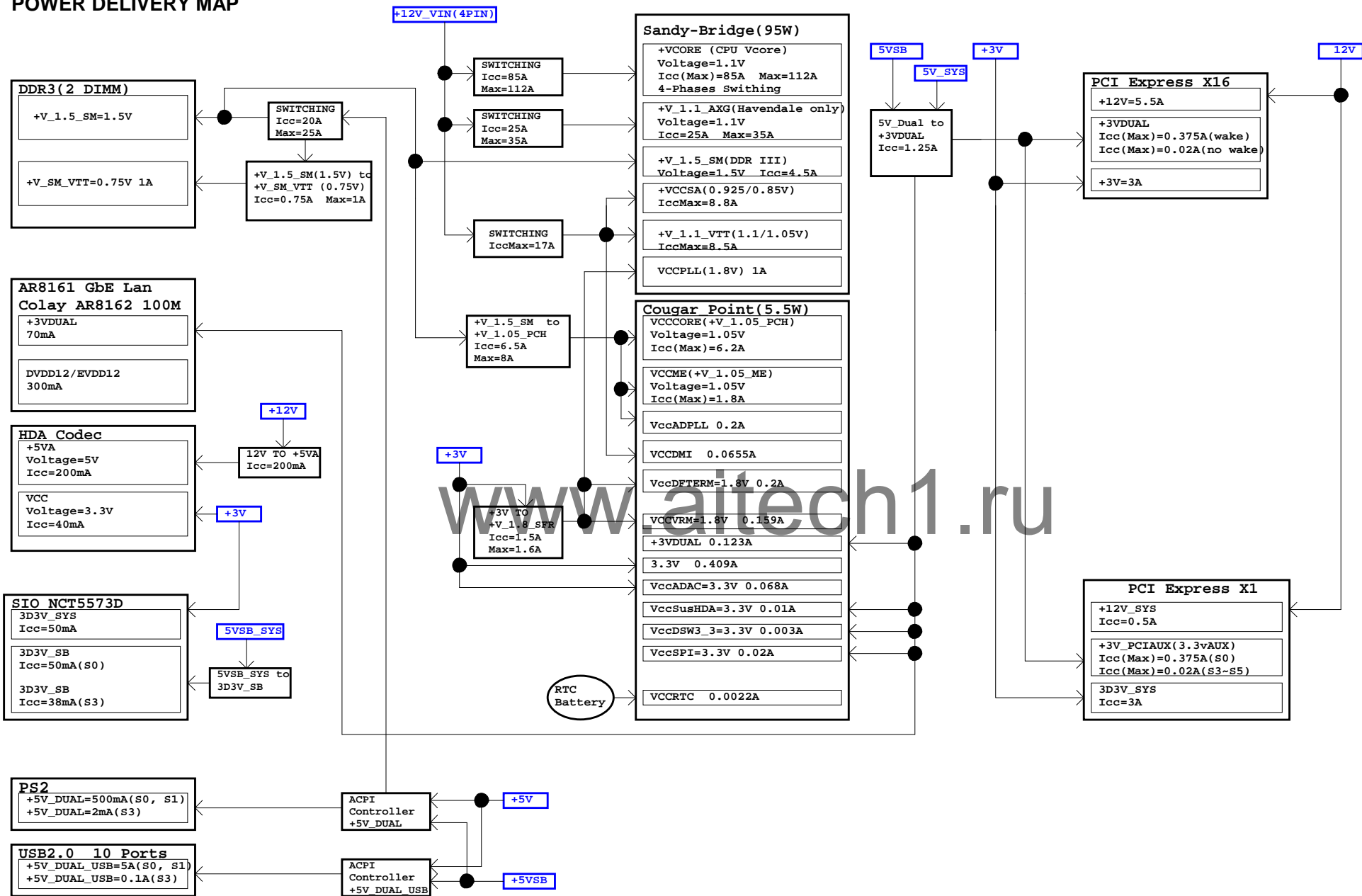
BLOCK DIAGRAM



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POWER DELIVERY MAP



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RESET / Power Good MAP

Sequence Signal Name:

- (1) O_PWRBTN#IN
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PSON#
- (4) B_ATX_PWROK
- (5) PCH_MEPWRGD
- (6) S_PCH_SYSPWROK P_VR_READY
- (7) PWRGD_3V
- (8) H_DRAMPWROK D3_RESET#
- (9) H_PWRGD
- (10) S_PLTRST# H_RESET#_R S_PLTRST#_R
- (11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
- (12) A_Z_RST#

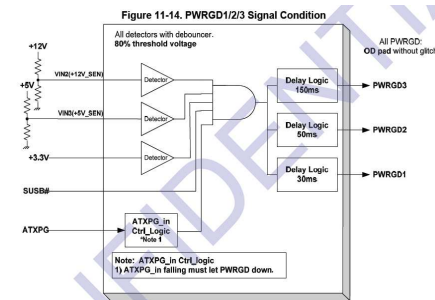
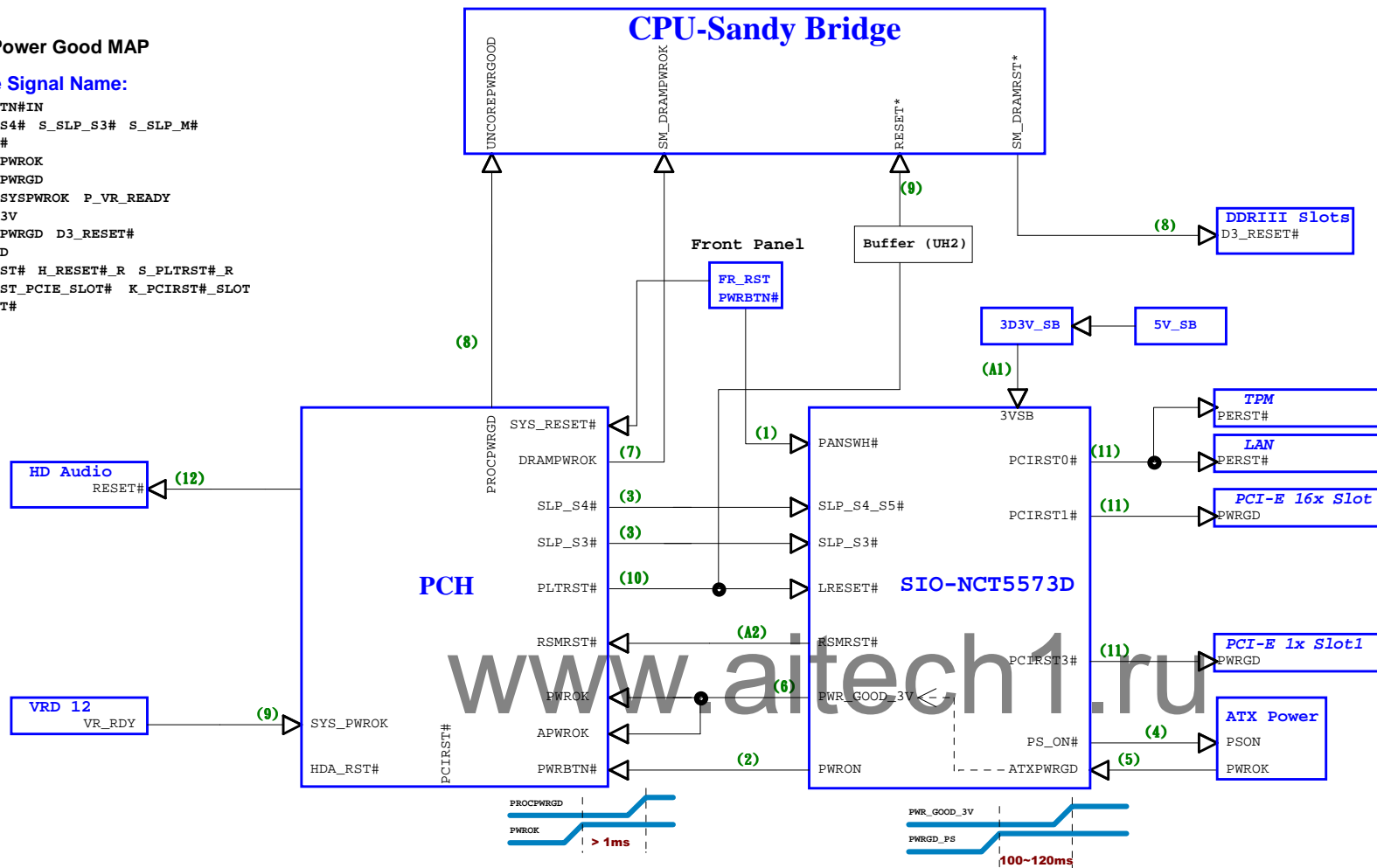


Figure 11-15. PWRGD1/2/3 Signal Timings

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IRQ Routing Table

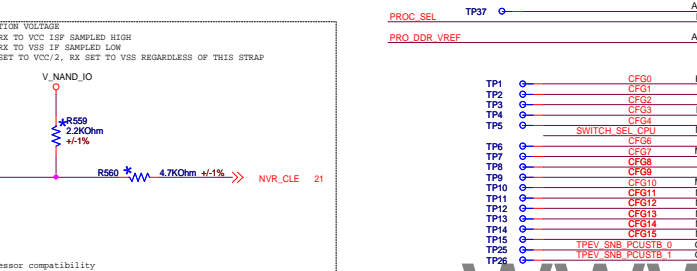
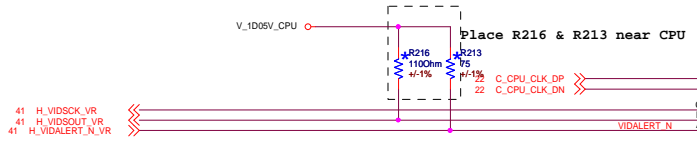
	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot1	A	B	C	D	16	0	0

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	B	C	D	A	17	2	2

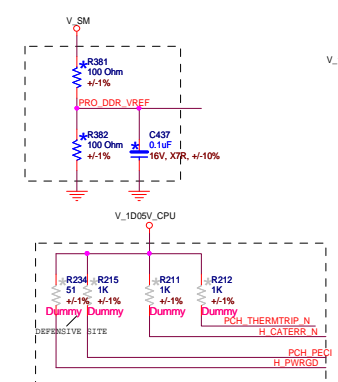
STRAPPING Table

CPU side		
CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default
		0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express
		01: reserved
		10: 2x8 PCI Express
		11: 1x16 PCI Express Default

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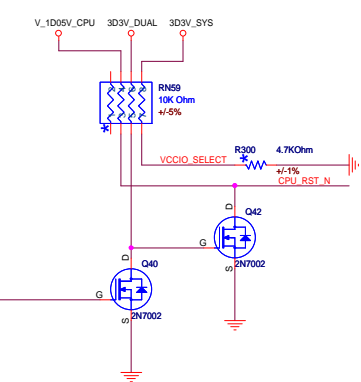
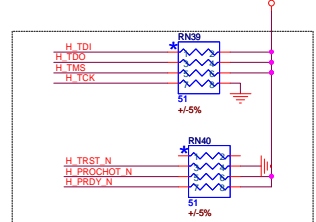
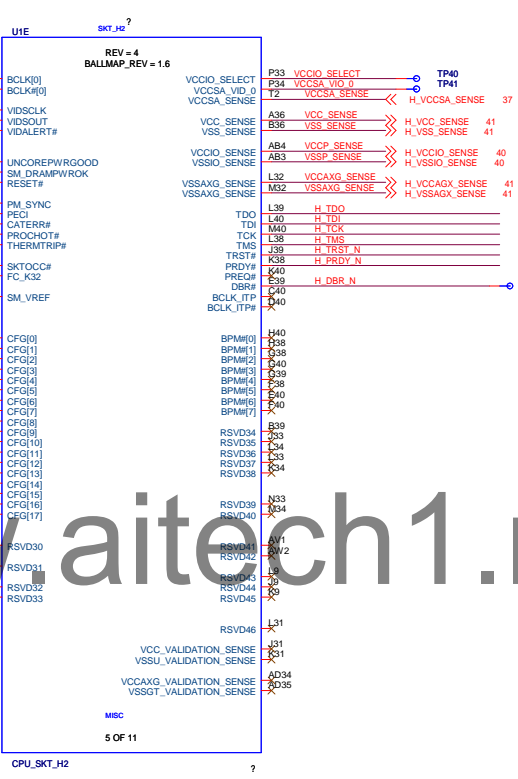
PLACE R381, R382, C437 IN SOCKET CAVITY



PLACE TDO TERMINATION
NEAR XDP CONNECTOR

TERMINATION IDEALLY TO BE
PLACED PLACE CLOSE TO EACH OTHER TO REDUCE STUB
NEXT TO IT OR WITHIN 1.5 OF CPU.

PLACE TEST* TERMINATION
ANYWHERE ON ROUTE.



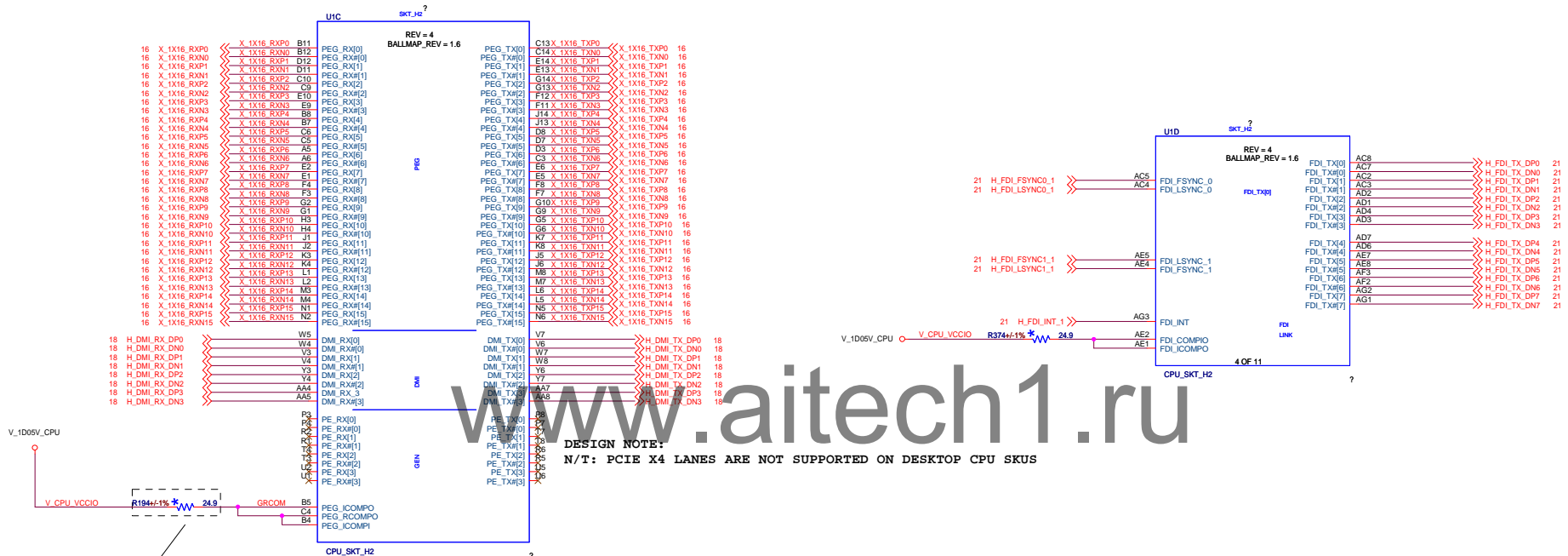
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Title CPU1-MSIC		
Size C	Document Number H61M06	Rev A
Date Thursday, January 05, 2012	Sheet 8	of 45



Short B4 & C4 together, route as a single 4 mil trace to R2
Route B5 to R2 as a separate 10 mil trace

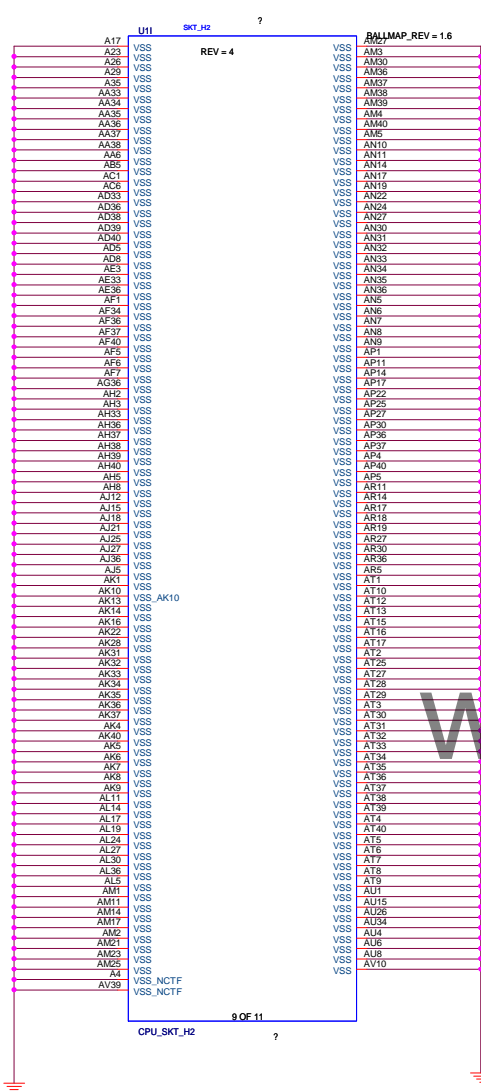
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Date Thursday, January 05, 2012	Sheet 9	of 45

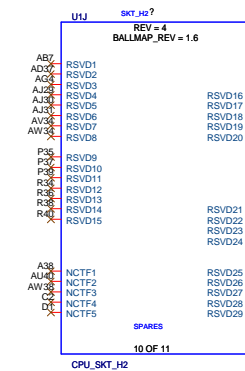
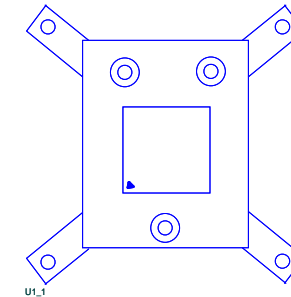


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Date: Thursday, January 05, 2012 Sheet 11 of 45



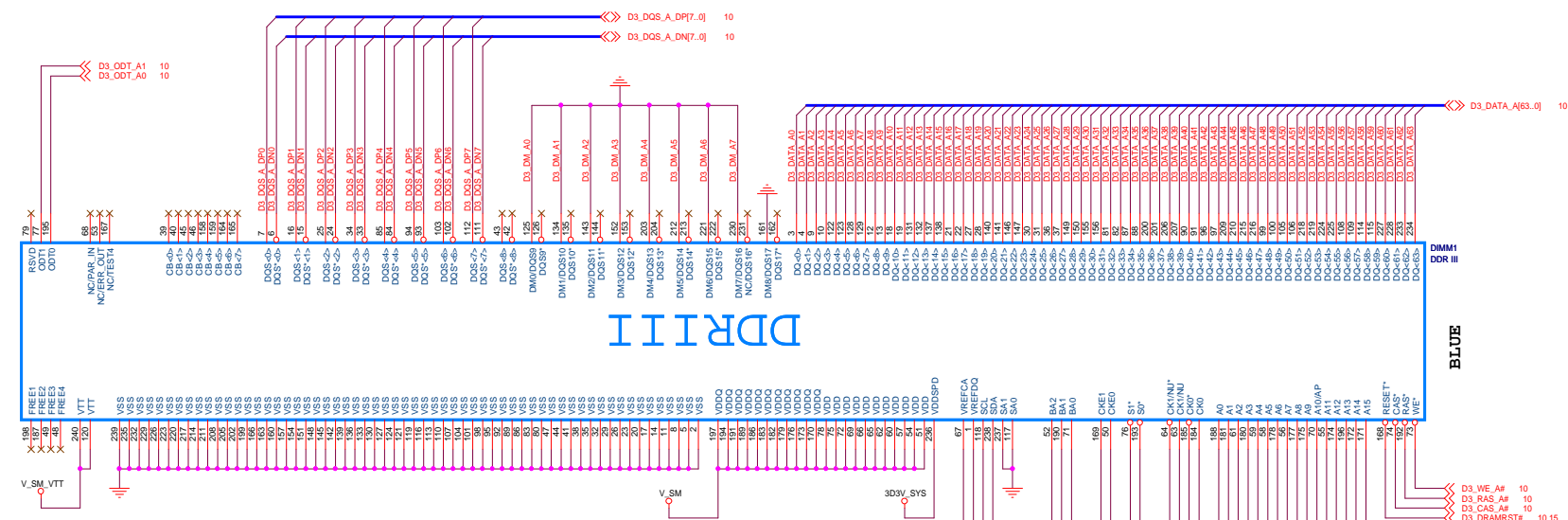
Fab 1.0



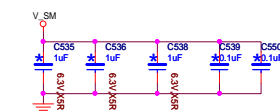
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Size C	Document Number H61M06	Rev A
Date Thursday, January 05, 2012	Sheet 13 of 45	

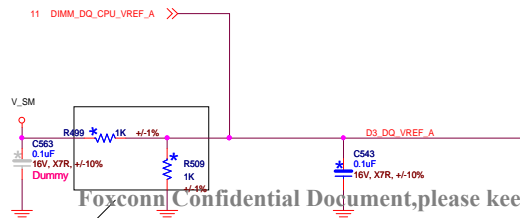
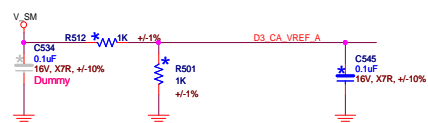
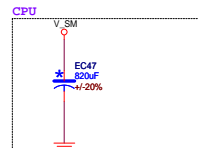
CHANNEL A DIMM 1
SMB ADDRESS:000



CLOSE TO DIMM POWER PIN

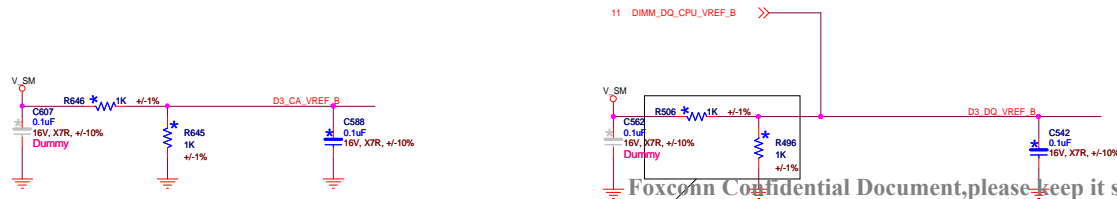
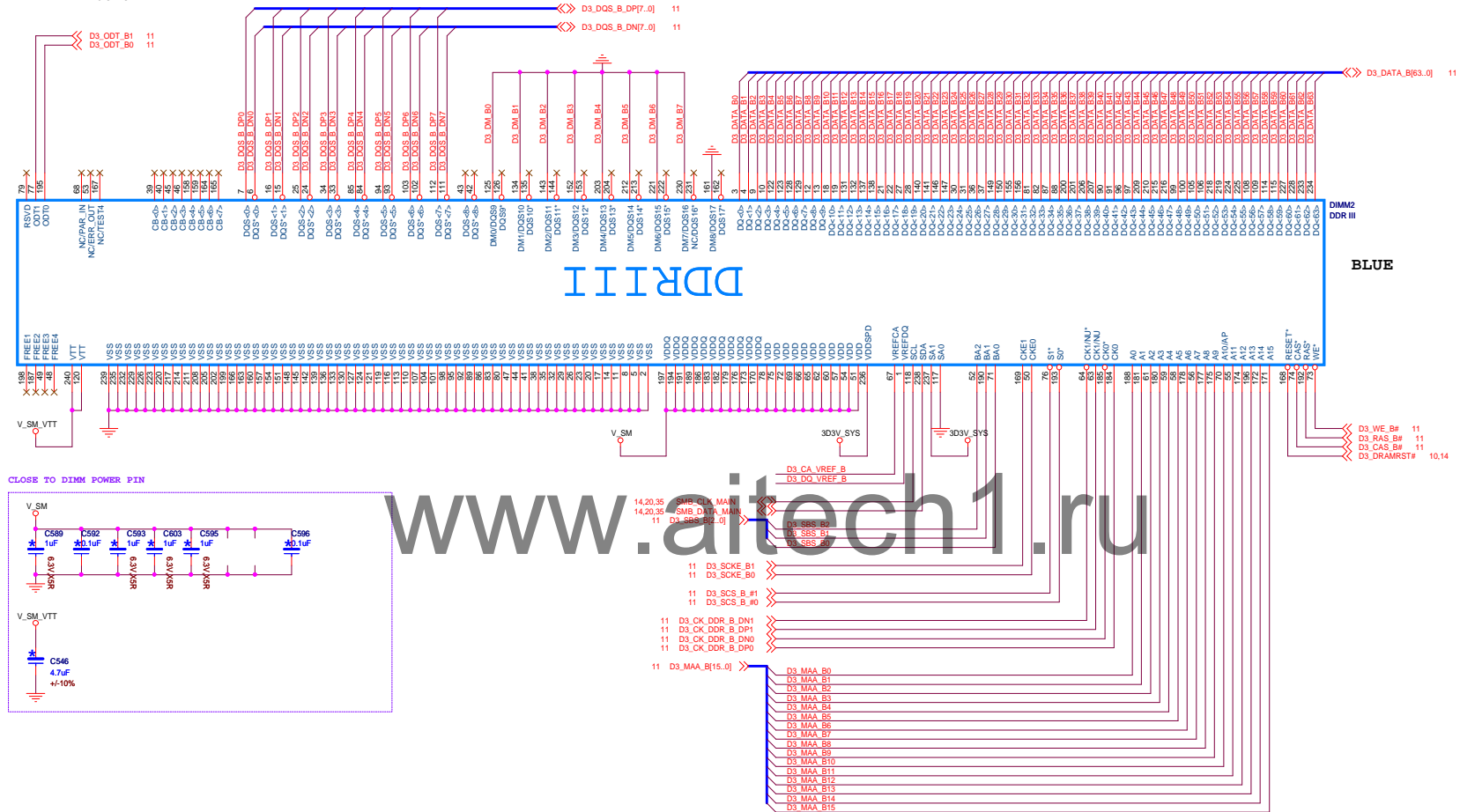


PLACE BETWEEN DIMM1 AND



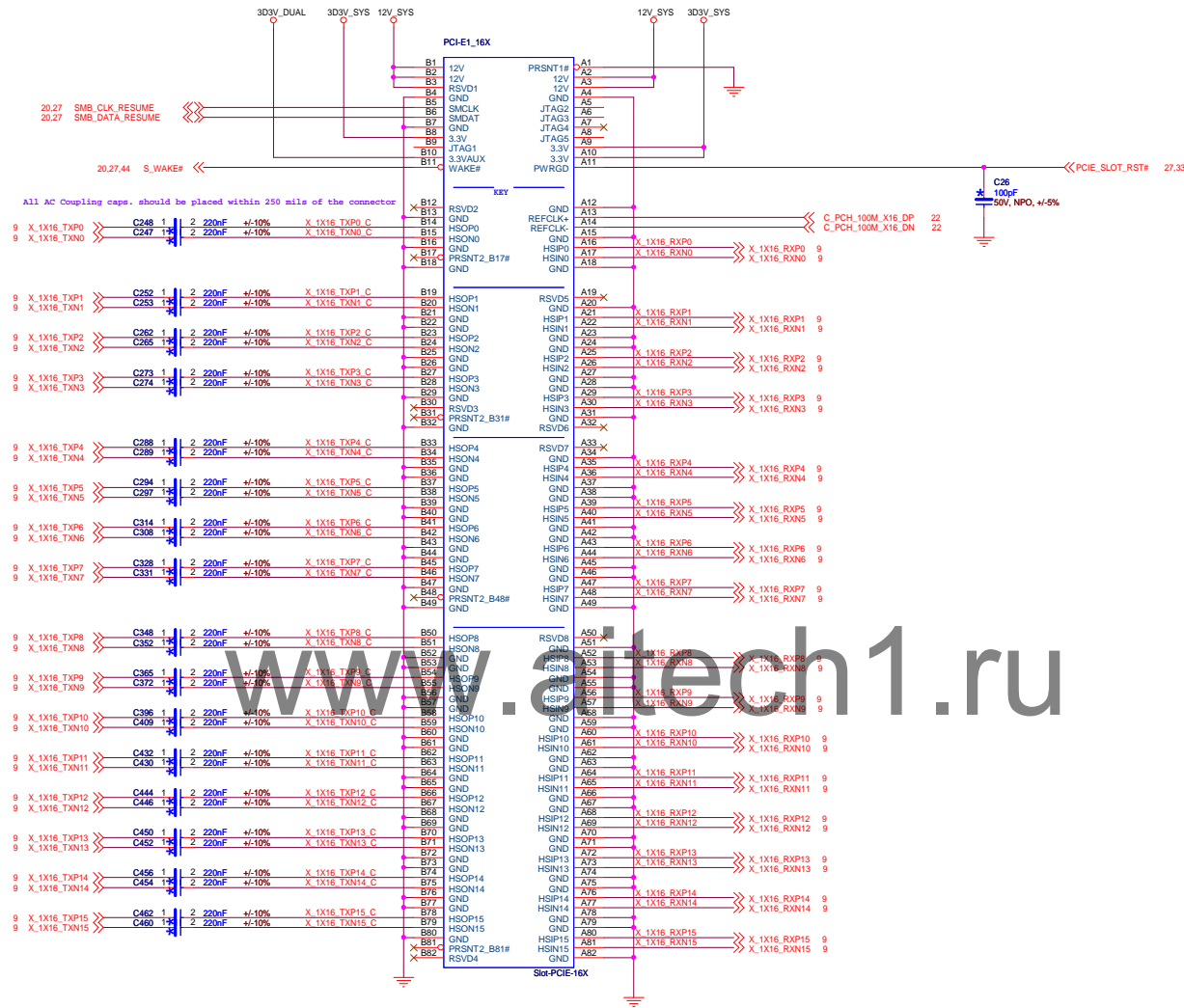
PLACE RESISTORS CLOSE TO CH_A DIMMS
ON DIMM_VREF_A

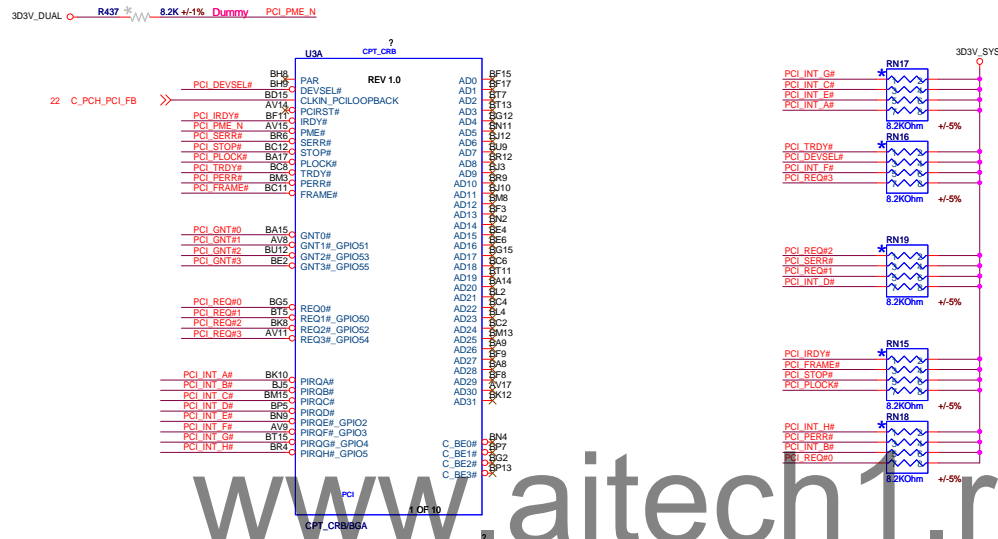
CHANNEL B DIMM 3
SMB ADDRESS:010



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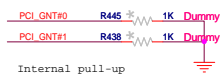
PLACE RESISTORS CLOSE TO CH_B DIMMS
ON DIMM_VREF_B



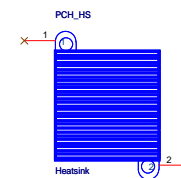


STRAP: Boot BIOSselect check whether GNT1 or SATA1GP(GPIO19)

BOOT DEVICE	GNT1	SATA1GP
LPC	0	0
NAND	0	1
PCI	1	0
SPI	1	1

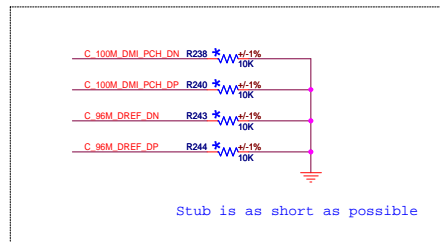
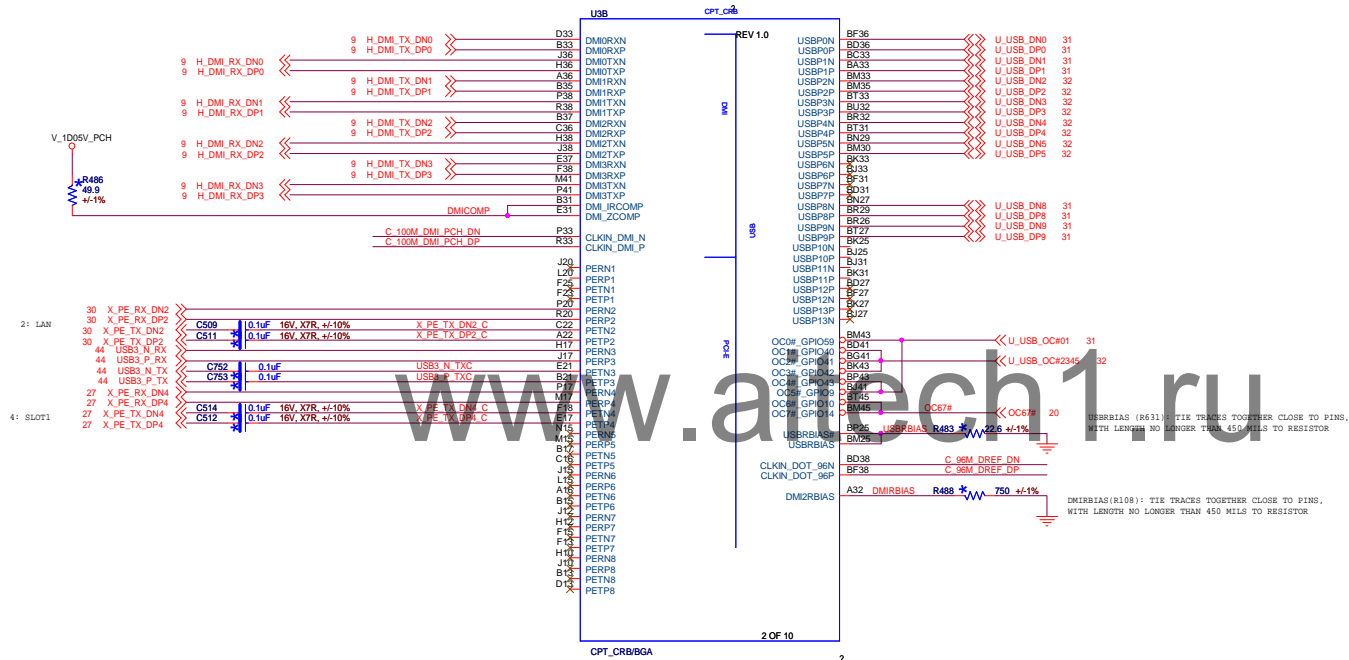


DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode
GNT2#/GPIO53:ESI strap for server platform
ONLY.Do not pull low.



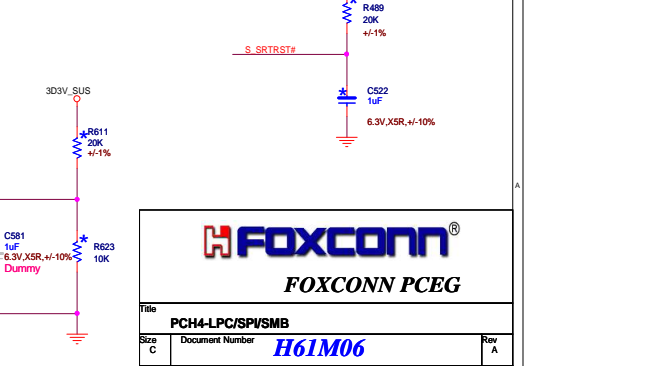
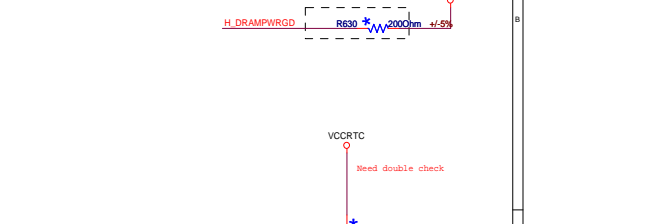
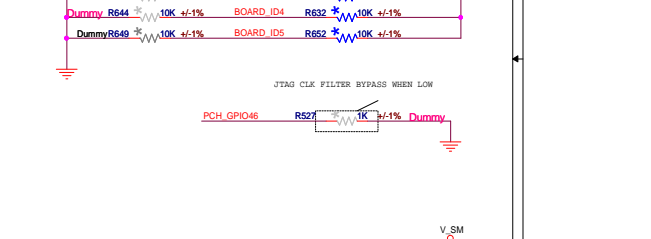
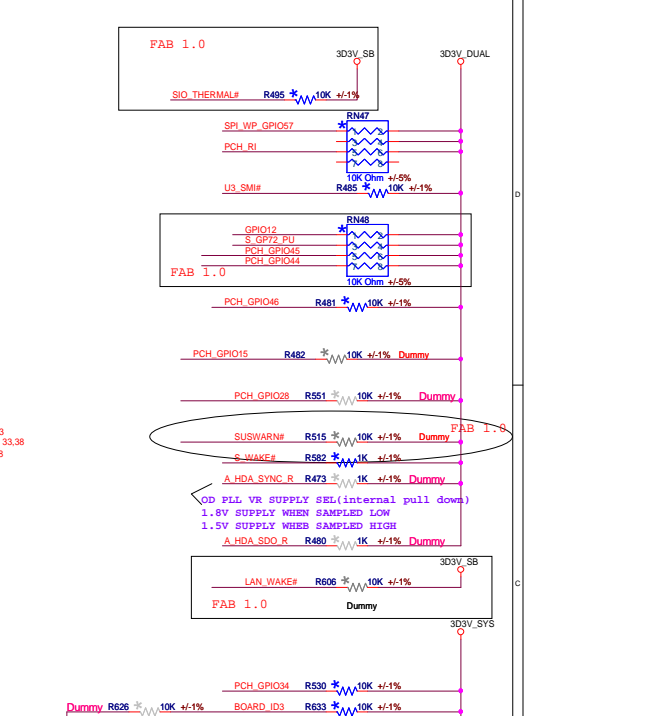
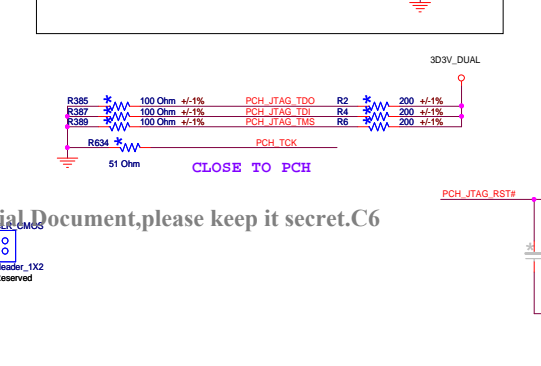
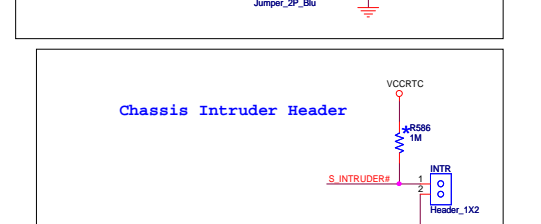
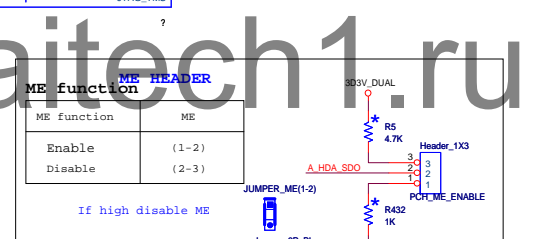
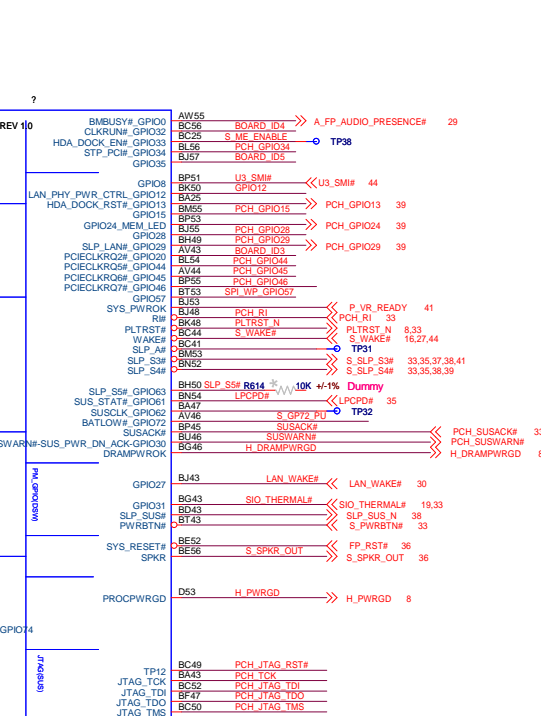
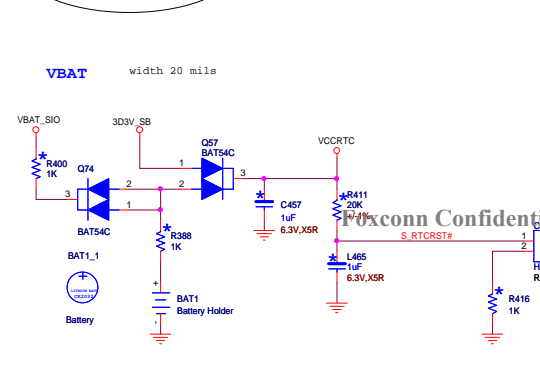
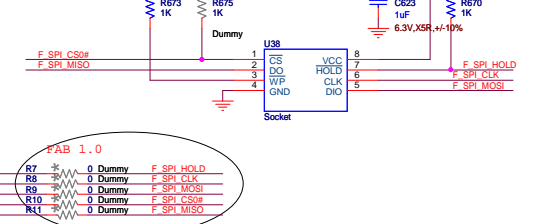
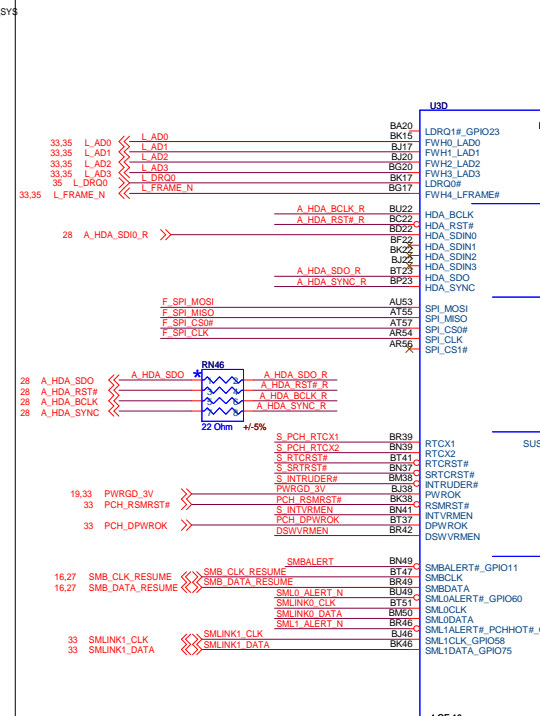
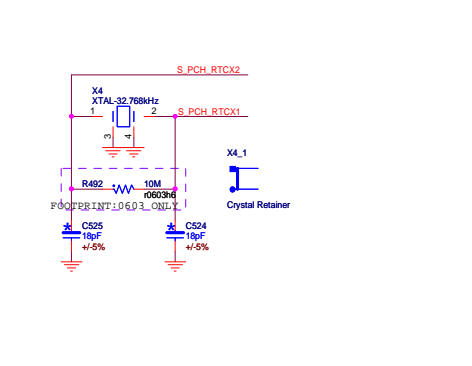
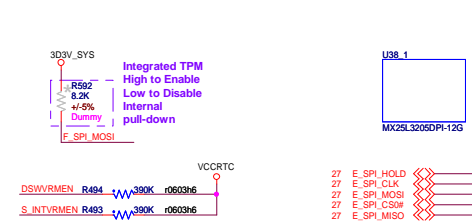
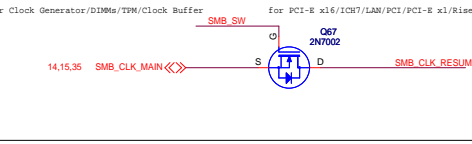
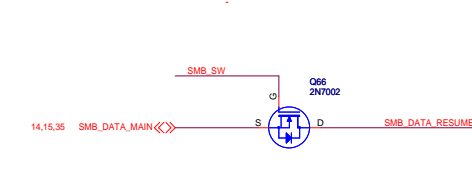
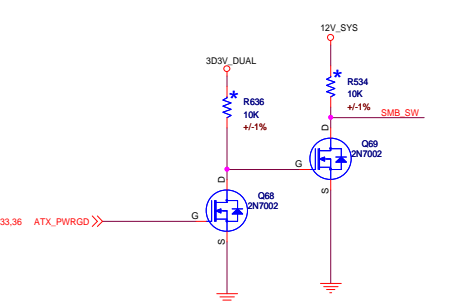
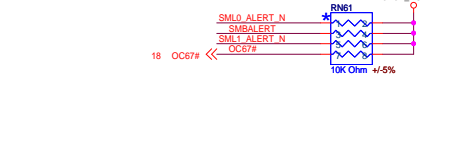
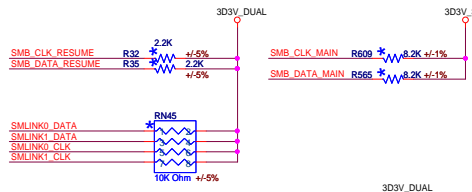
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Date: Thursday, January 05, 2012	Sheet 17	of 45



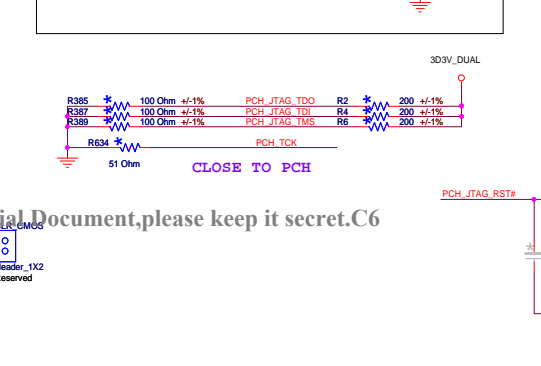
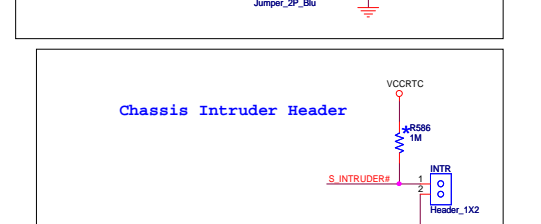
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Date Thursday, January 05, 2012	Sheet 18	of 45



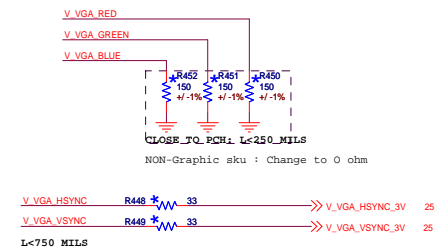
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ME function	ME
Enable	(1-2)
Disable	(2-3)

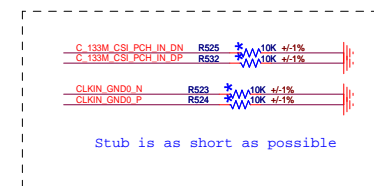



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Size	Document Number	H61M06	
Date:	Thursday, January 05, 2012	Sheet	20 of 45

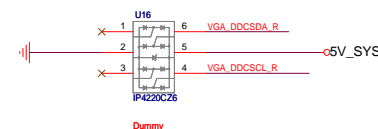
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Size	Document Number	H61M06	Rev A
Date:	Thursday, January 05, 2012	Sheet	21 of 45



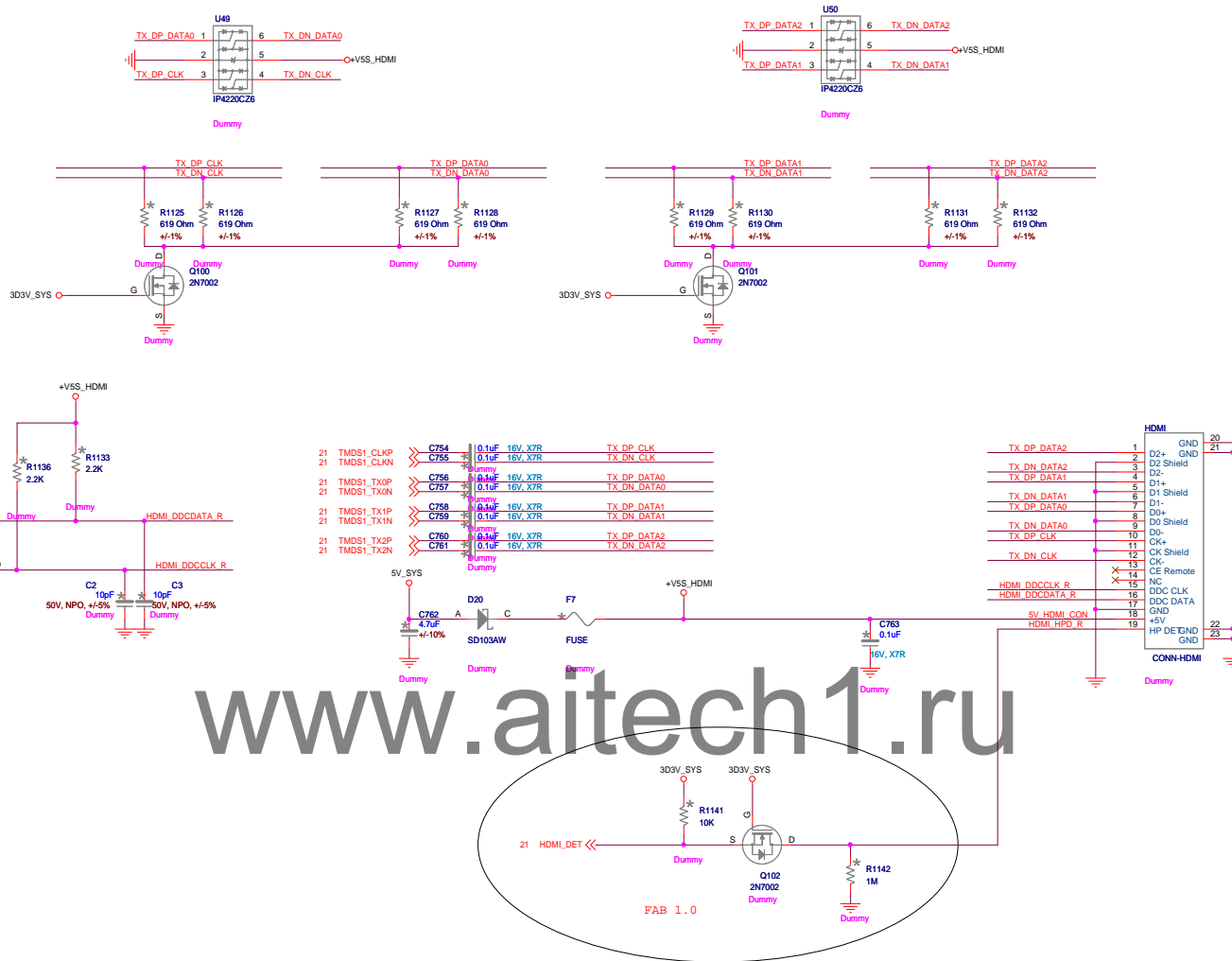
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Size	Document Number	H61M06	Rev
			A
Date:	Thursday, January 05, 2012	Sheet	22 of 45





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VGA				
Size	Document Number	Sheet		Rev
C	H61M06			
Date	Thursday, January 05, 2012	Sheet	25	of 45

HDMI Connector

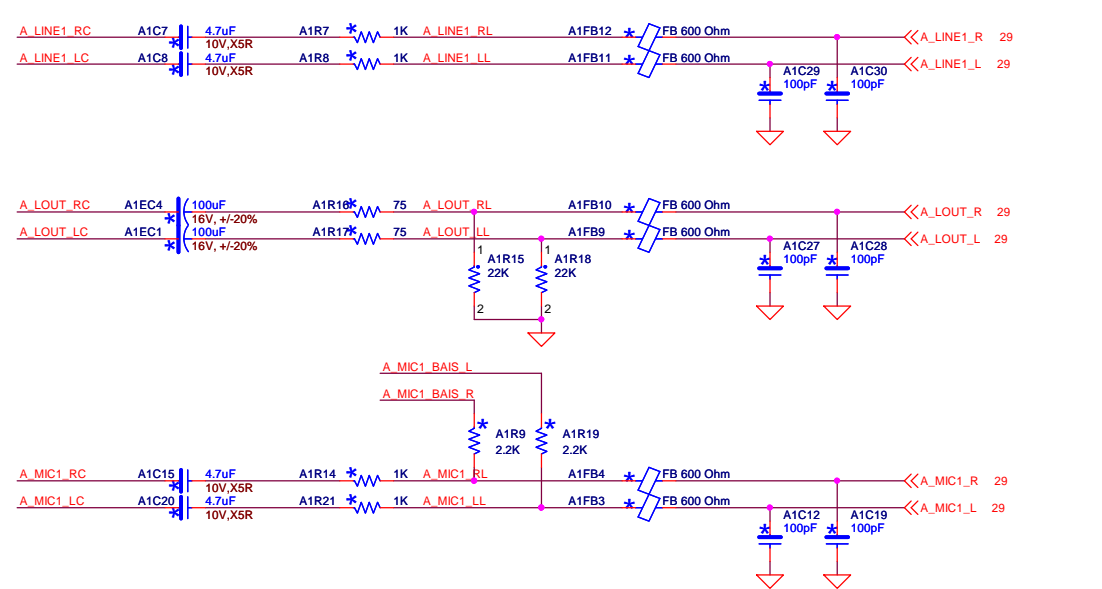
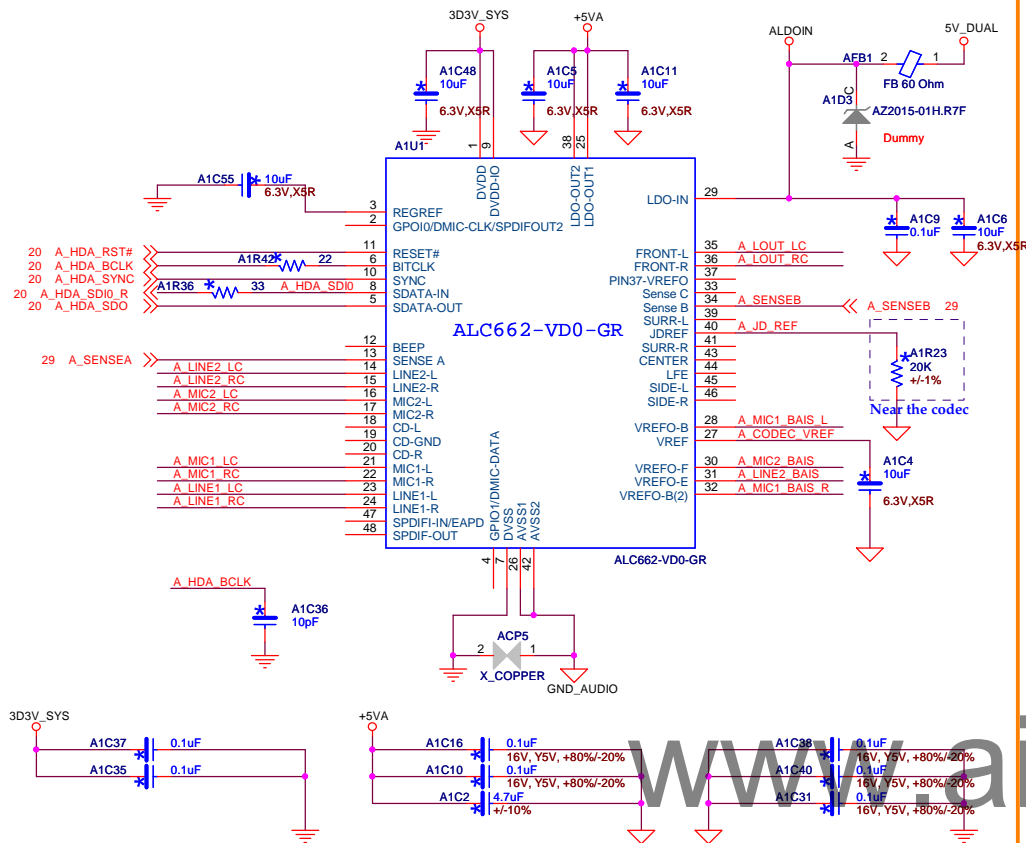


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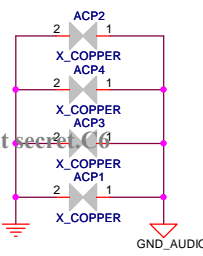
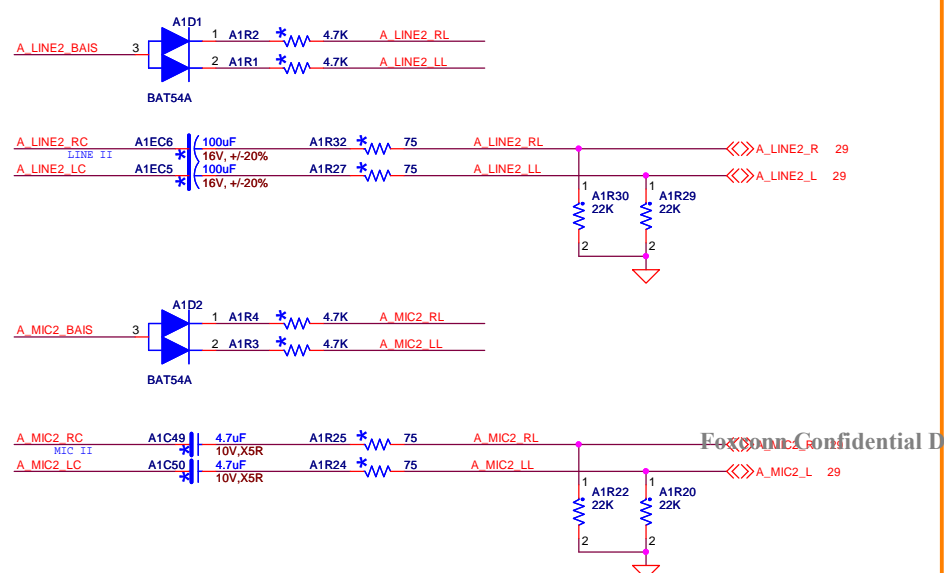
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Size C	Document Number H61M06	Rev A
Date Thursday, January 05, 2012	Sheet 27	of 45



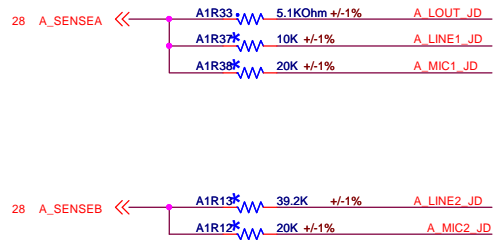
FRONT PANEL



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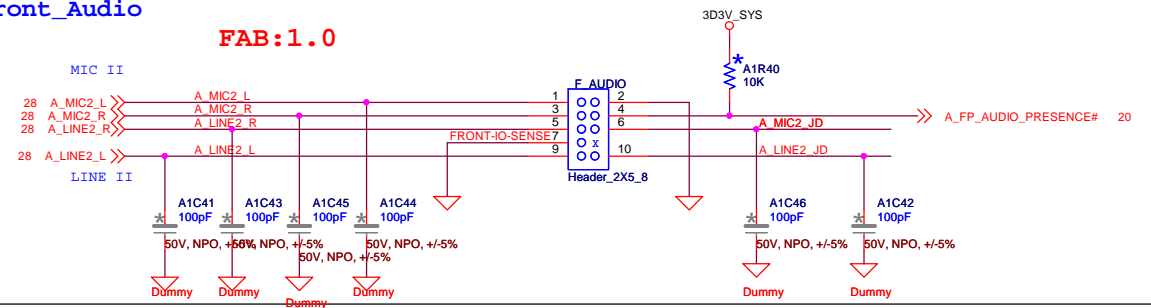
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Date:	Thursday, January 05, 2012	Sheet	28 of 45

JACK SENSE



Front_Audio

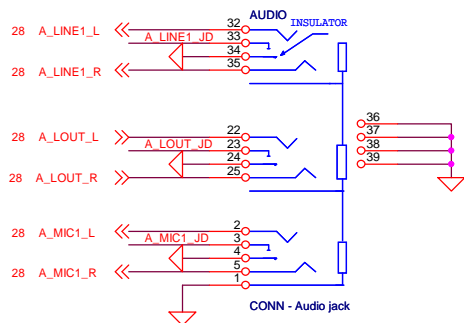
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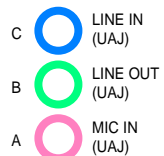
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+5VA for AUDIO

Audio Jack



Audio Jack



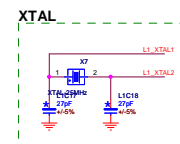
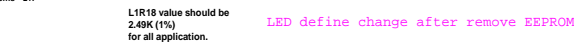
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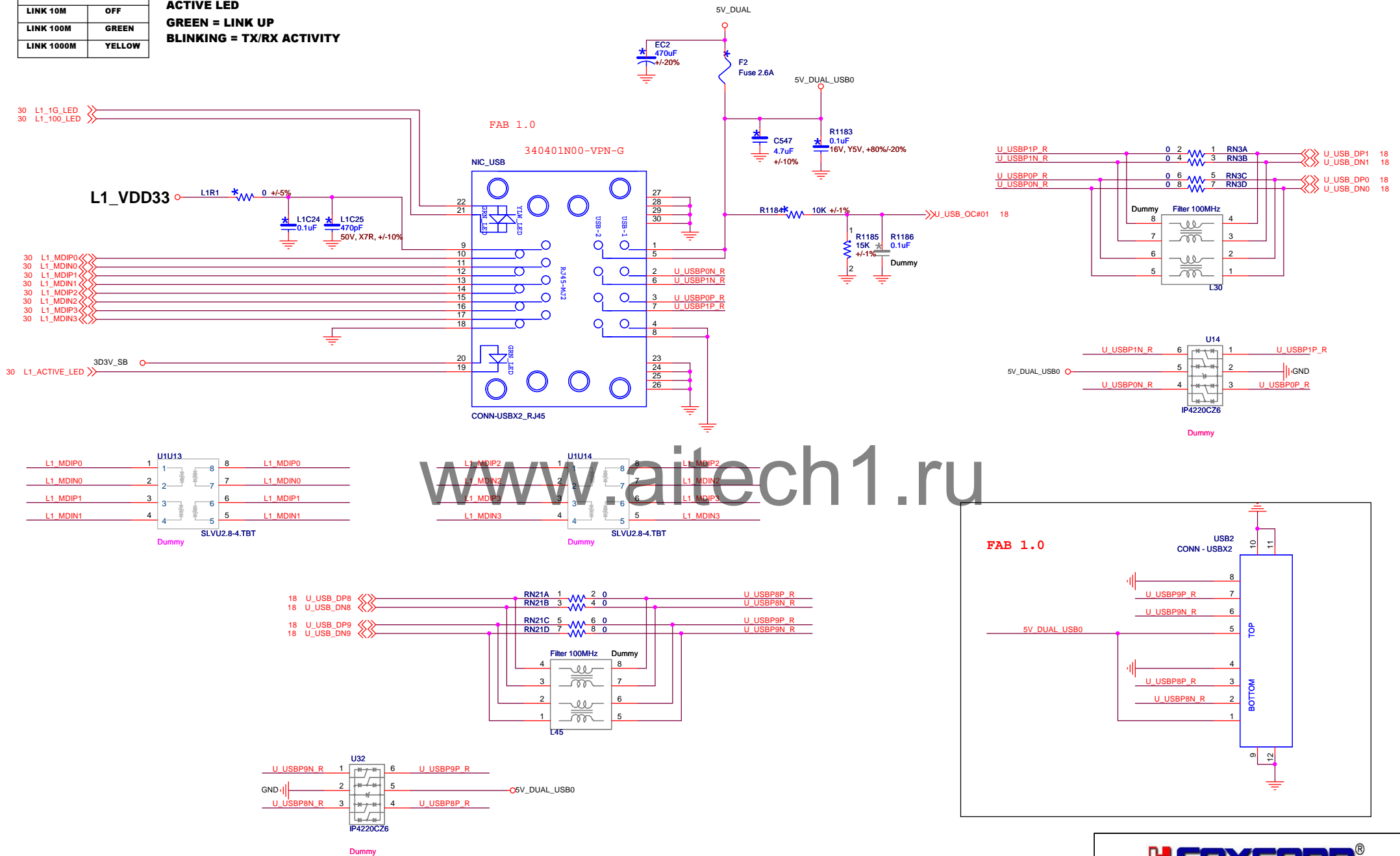
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Size	A3	Document Number	H61M06
Date:	Thursday, January 05, 2012	Sheet	29 of 45
Rev	A		

Remove For Disable Switch Regulator (Accept External 1.85V Power Supply)



ACTIVE LED
GREEN = LINK UP
BLINKING = TX/RX ACTIVITY



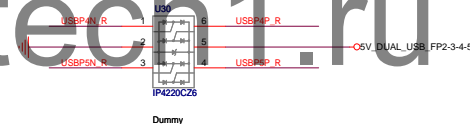
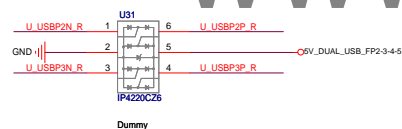
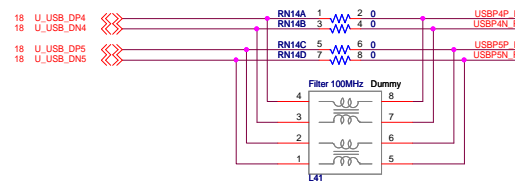
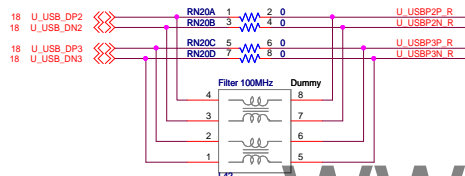
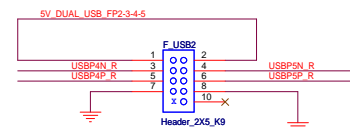
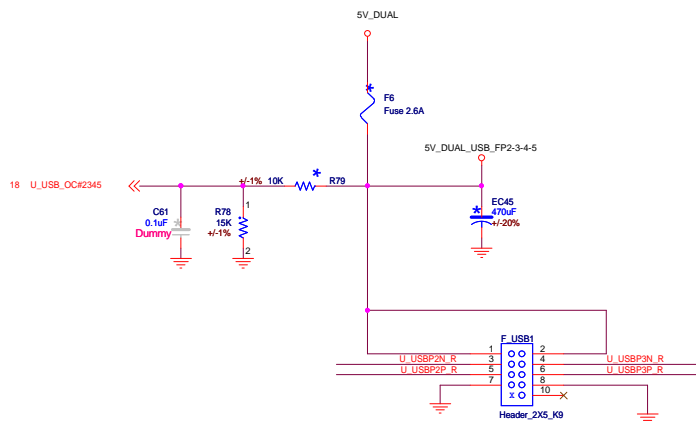
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Date:	Thursday, January 05, 2012	Sheet	31 of 45

Front_USB2



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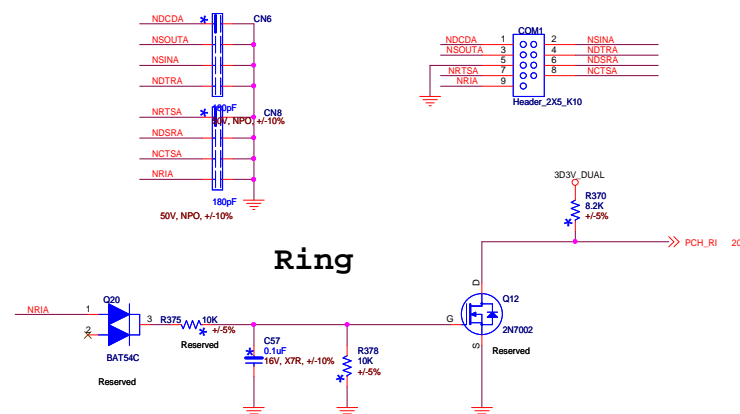
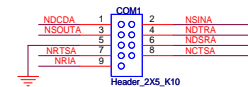
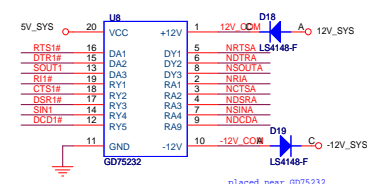
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Front USB2.0 Header			
Size	Document Number		Rev
C	H61M06		A
Date:	Thursday, January 05, 2012	Sheet	32 of 45

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP(default)
Pin-23		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK(Default)
Pin-57		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 6th/73th default = 80h
Pin-59		0	EC Index 6th/73th default = 00h
JP4	KSPWR_EN	1	Disable KSPwr Sequence(Default)
Pin-61		0	Enable KSPwr Sequence

```

1.Pin 6:ATXPG
2.Pin 30:SUSB#
3.Pin Pin 23 / Pin 57/ Pin 59/ Pin61
4.Pin38-41 KCLK/KDAT/MCLK/MDAT
5.Pin 63 pull high to 3VSB

```

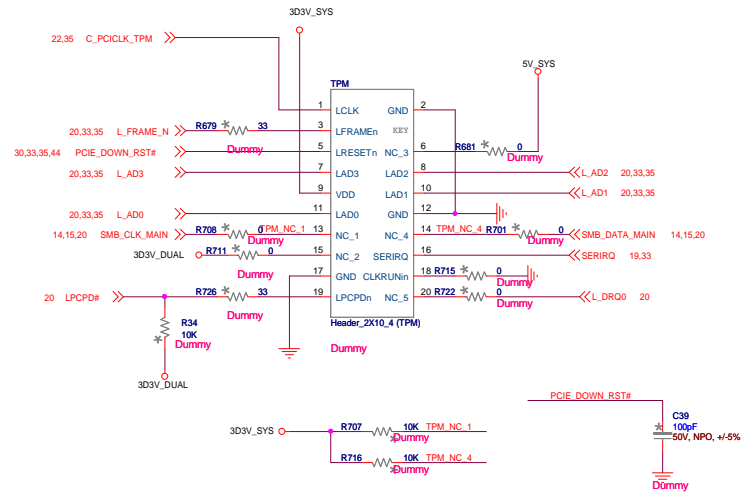


RIS
*CV
PCF SUSAC#
XX
PMI SUSAC#
3

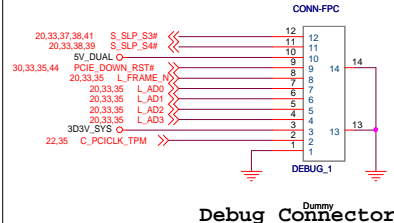


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Size C	Document Number H61M06	Rev A	
Order: Thursday, January 06, 2011 8:00pm 22 of 46			

TPM



LPT PORT



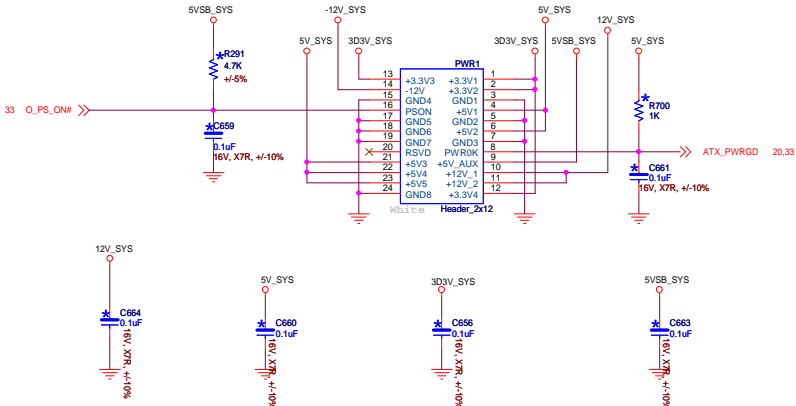
COM HEADER

COM PORT

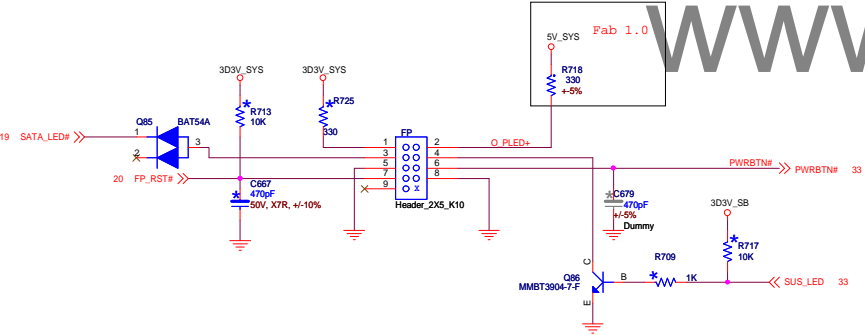
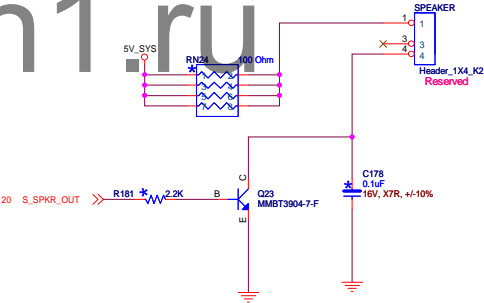
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ATX POWER CONNECTOR



BUZZER/Speaker Header

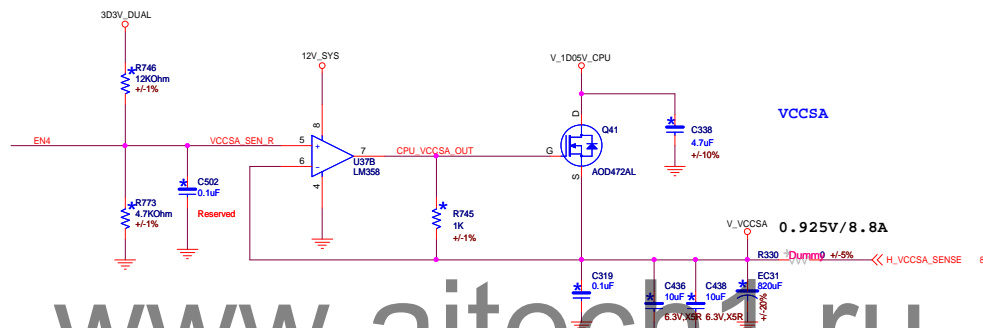
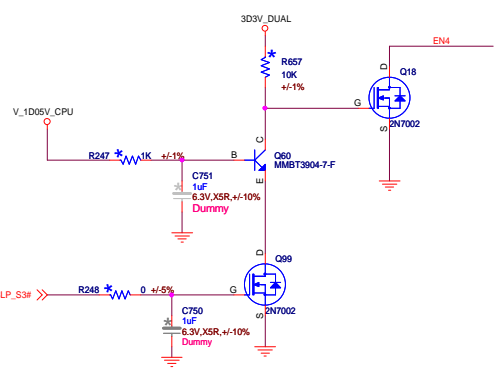
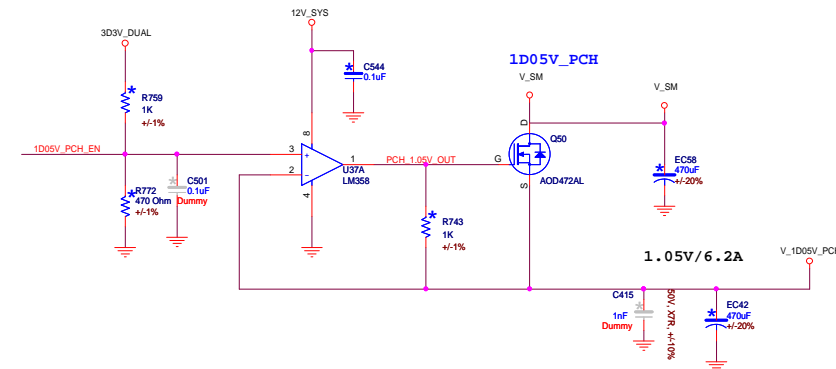
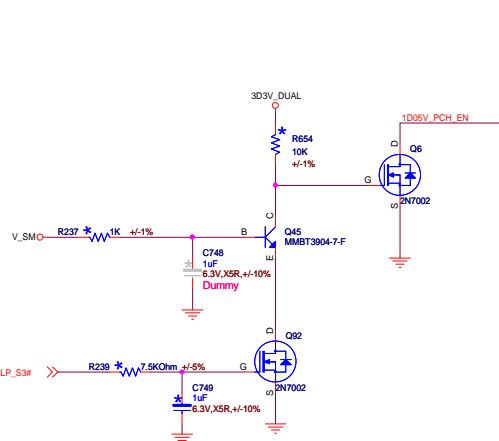


Front Panel Switch/LED					
HD_LED+	1	2	Power		
HD_LED-	3	4	Power LED(Green)		
GND	5	6	Power button		
Reset button	7	8	Detect pin		
Detect pin	9	10	Key		

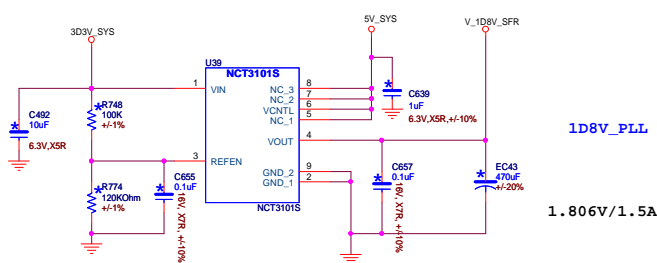
Front I/O Header

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Pull lo for 0.9V vref out and address 54h

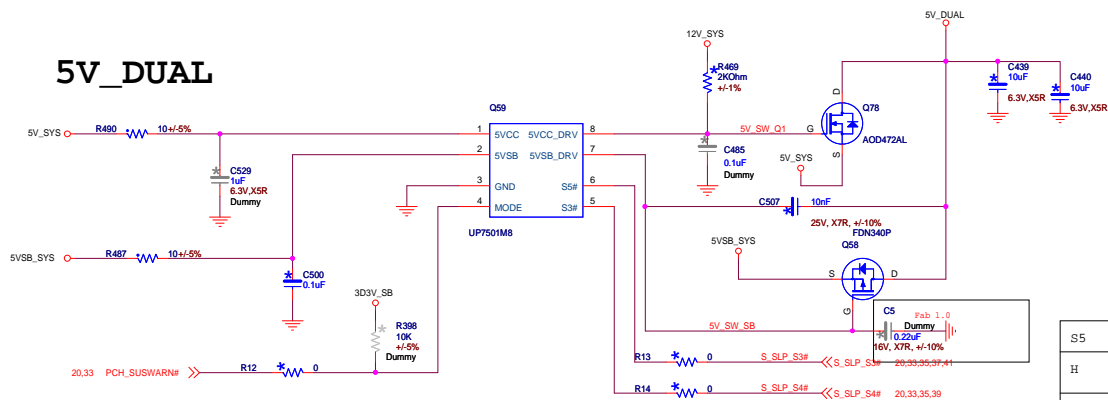


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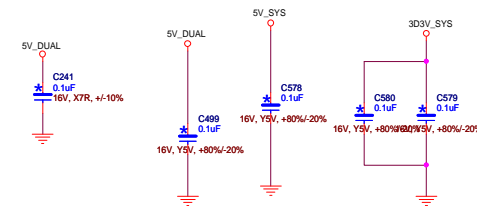
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5V DUAL



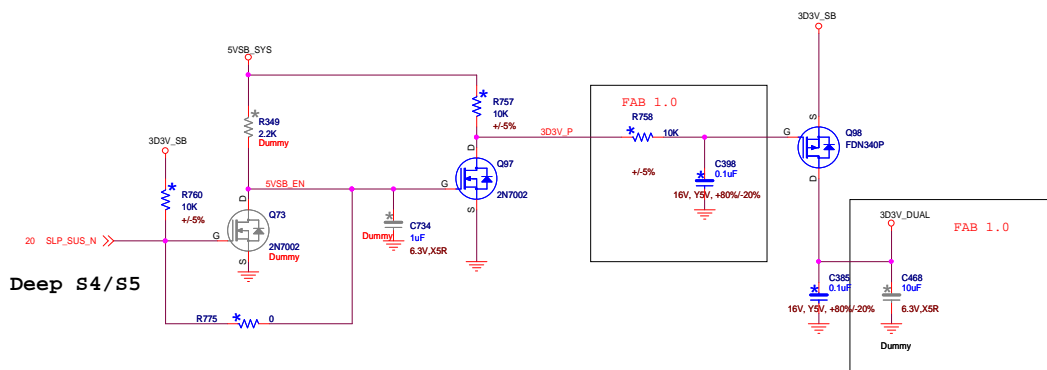
HI= S4/S5 5VDUAL FORM 5VSB
Low= S4/S5 5VDUAL TURN OFF

S5	S3	NODE	5VDUAL
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown

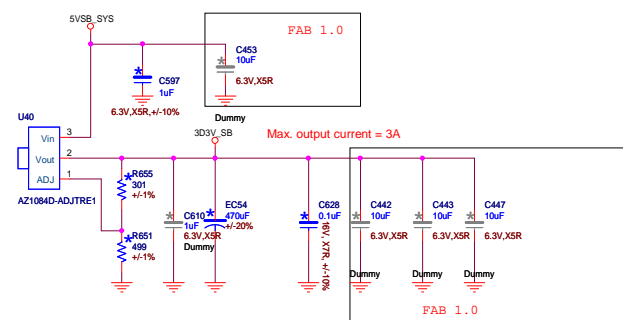


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3D3V_DUAL



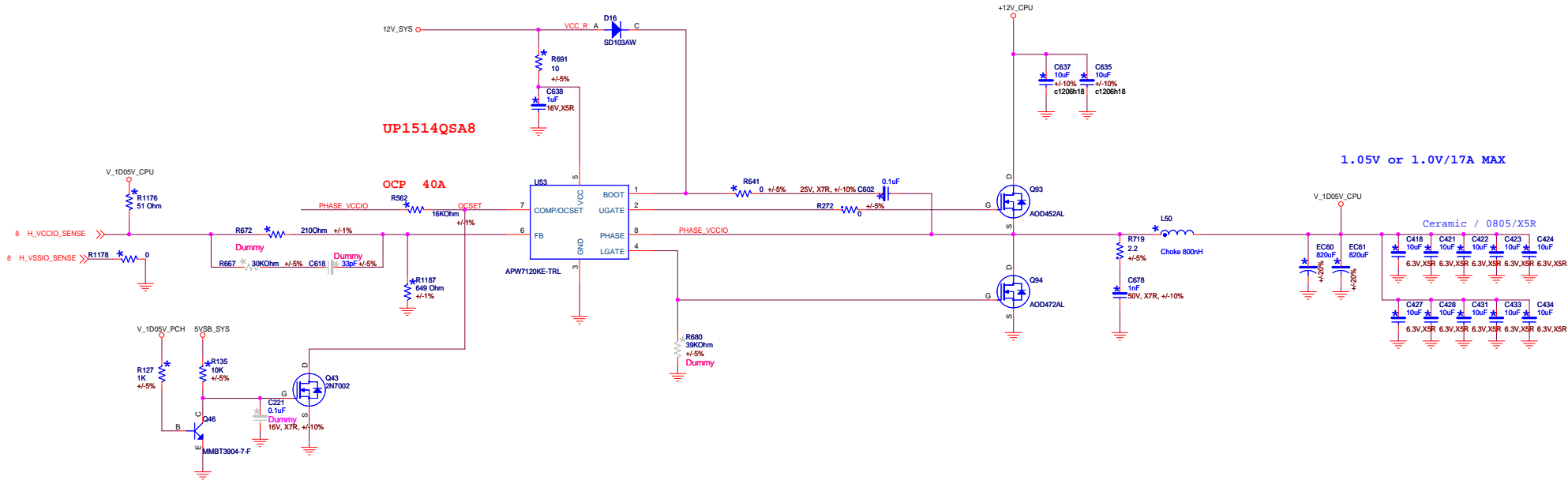
3D3V_SB



Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V

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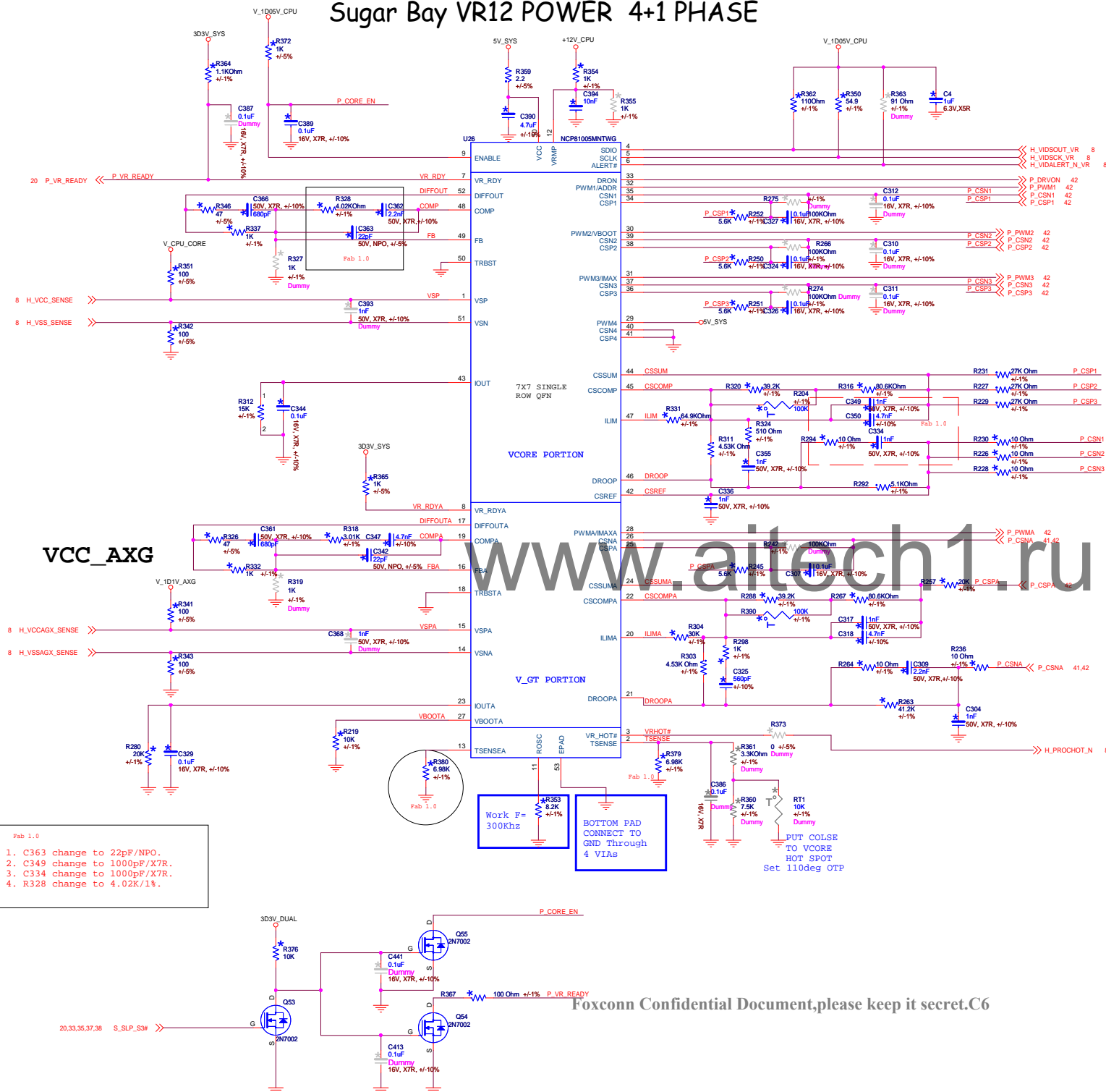


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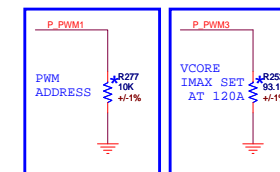
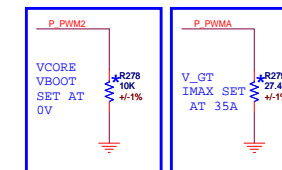
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FOXCONN® FOXCONN PCEG			
Title CPU_VCCIO			
Size C	Document Number H61M06	Rev A	
Date: Thursday, January 05, 2012	Sheet 40	of 45	

Sugar Bay VR12 POWER 4+1 PHASE



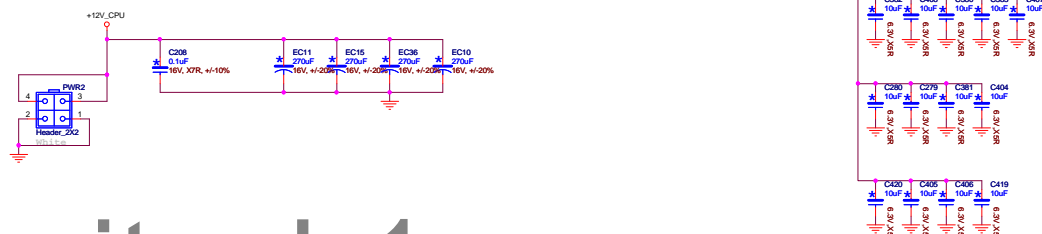
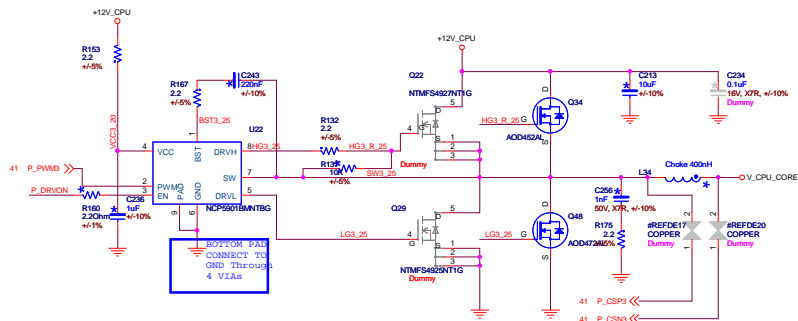
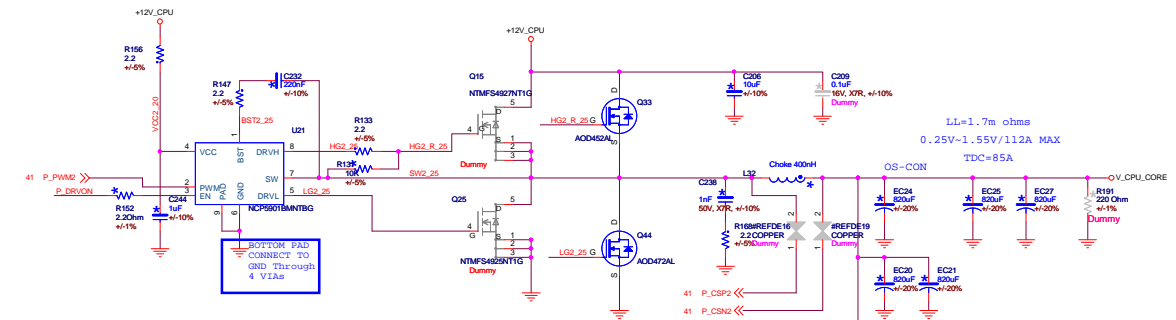
VCC_CORE



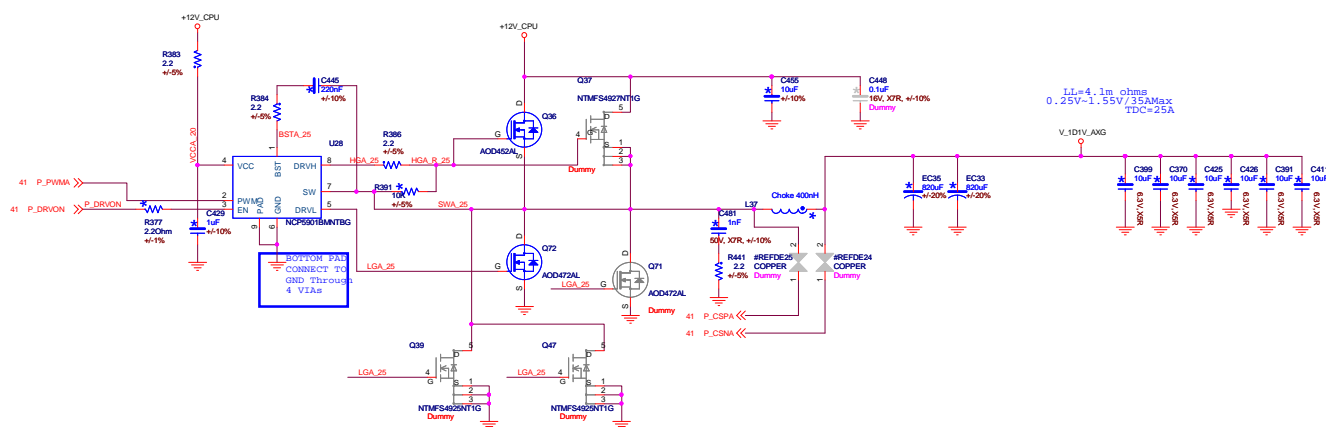
BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1.0V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V

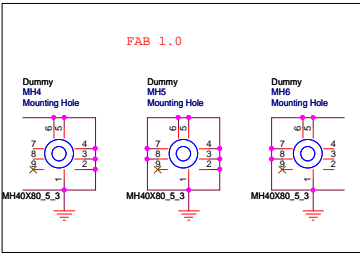
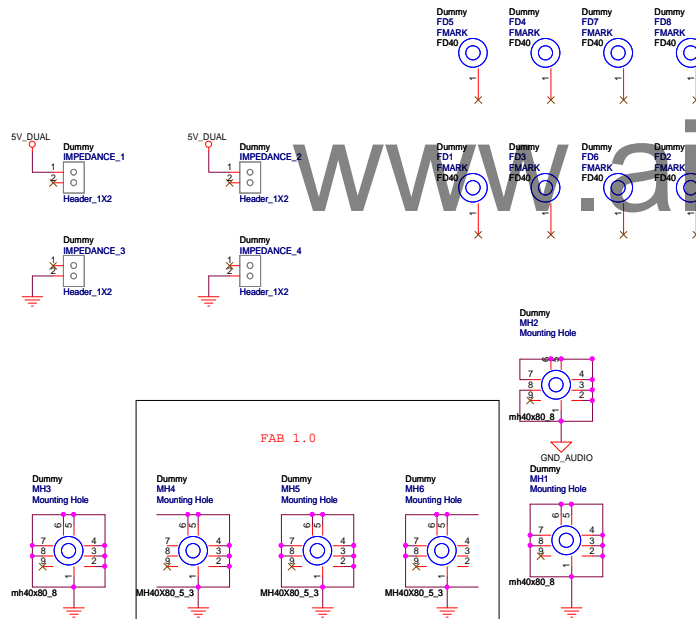
PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

READY
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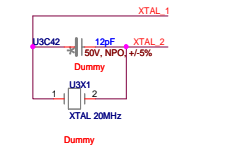
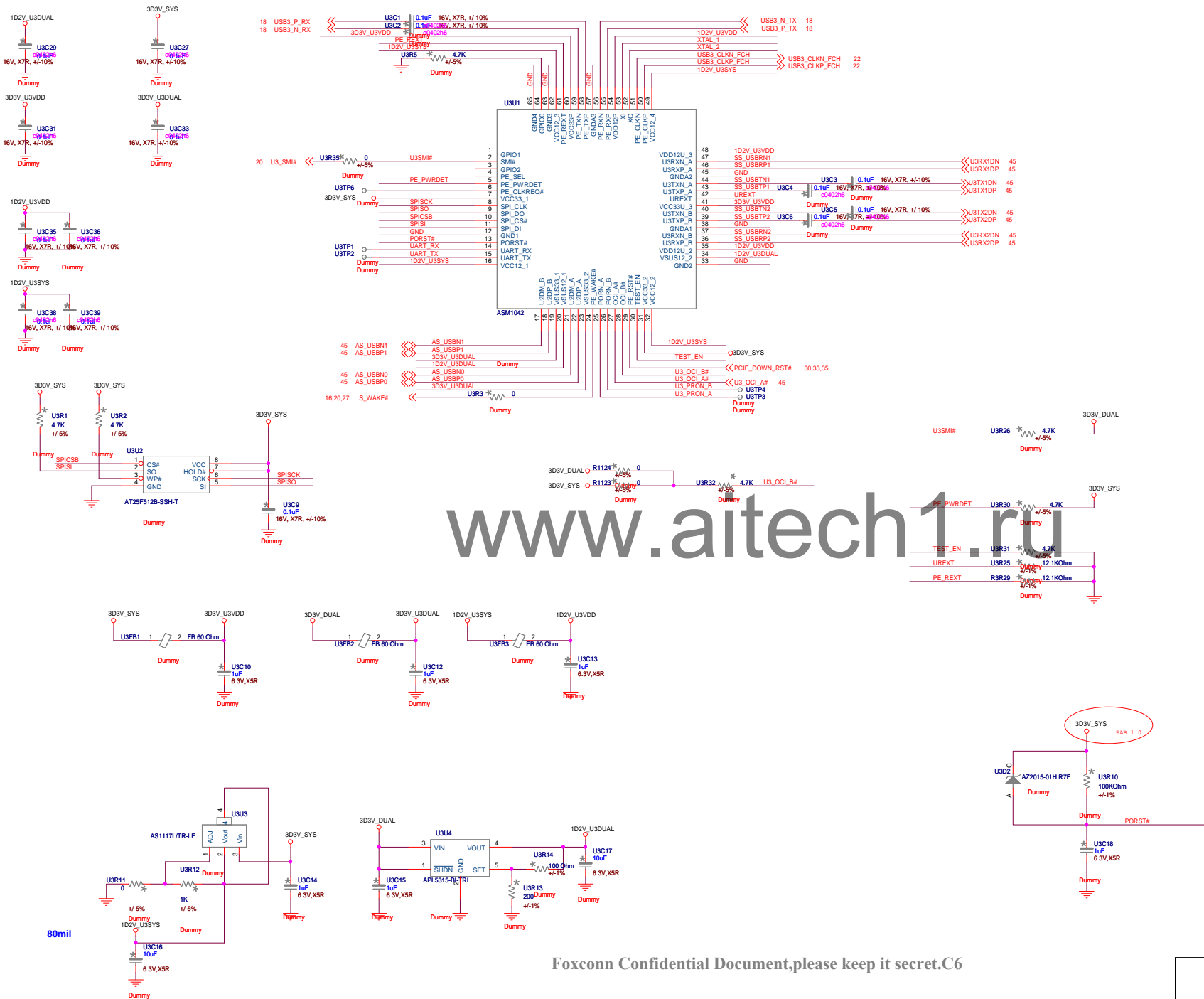


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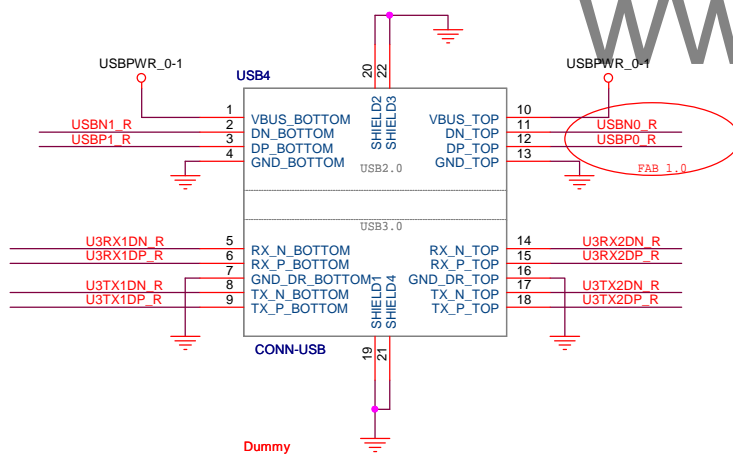
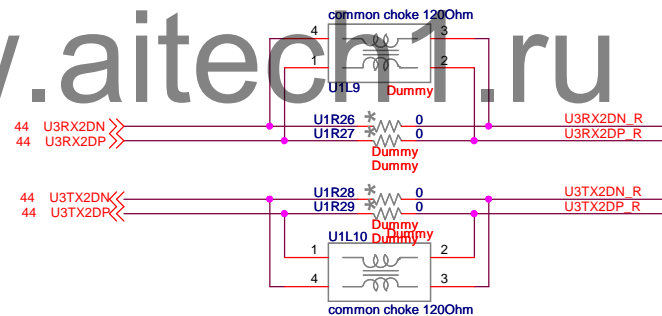
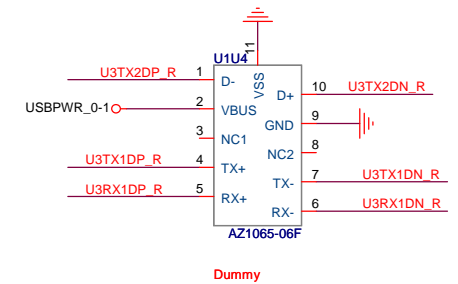
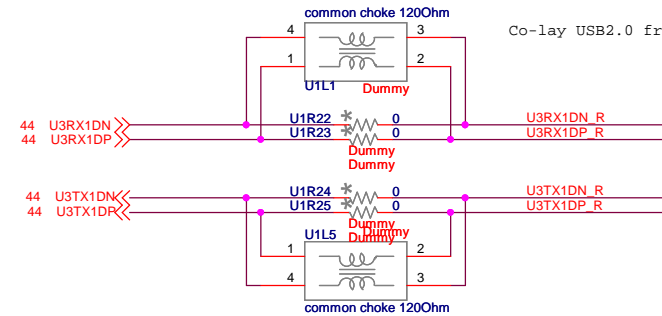
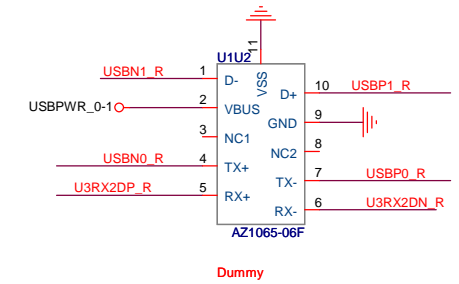
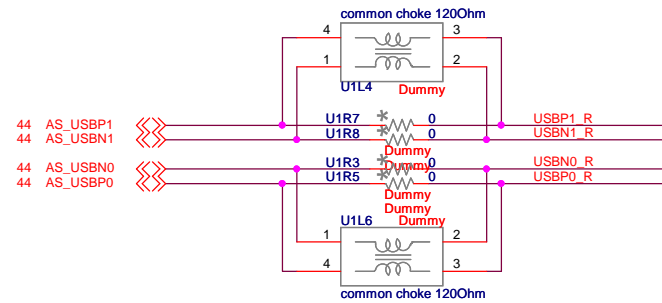
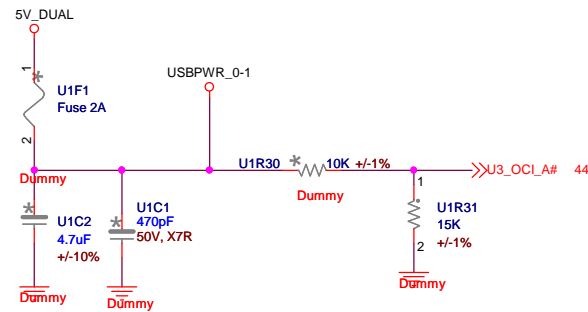


Pin44-XTAL2 is External Clock Input Pin.

FAB 1.0



File		
USB3		
Size	Document Number	Rev
C	H61M06	A
Date:	Thursday, January 05, 2012	Sheet 44 of 45



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Title			
USB PORT			
Size B	Document Number <i>H61M06</i>		Rev A
Date:	Thursday, January 05, 2012	Sheet 45 of 45	